Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.880-881

B-9-2

Reliability and Memory Characteristics of Sequential Laterally Solidified LTPS TFT with a ONO Stack Gate Dielectric

Ssu-I Hsieh and Ya-Chin King

Microelectronics Lab., STAR Group, Department of Electrical Engineering
National Tsing-Hua University, Hsin-Chu, Taiwan, R.O.C
TEL: 886-3-5715131 ext4034, FAX: 886-3-5721804, e-mail: sihsieh@well.ee.nthu.edu.tw

Hung-Tse Chen, Yu-Cheng Chen, Chi-Lin Chen, and Jia-Xing Lin

Electronics Research and Service Organization
Industrial Technology Research Institute, Hsin-chu, Taiwan, R.O.C.,
TEL: 886-3-5913538, FAX: 886-3-5820052, e-mail: HTChen@itri.org.tw

1. Introduction

Low temperature poly-Si (LTPS) TFTs exhibit high mobility and driving current, making them a preferred for peripheral circuit implementation on AMLCD and AMOLED. In order to realize high performance TFTs, it is effective to use thin gate dielectrics. A thinner gate dielectric can also result in higher electric storage capacity, which enables storage capacitor area in pixel to be reduced; the aperture ratio of pixel can therefore be increased. Thus, the brightness and color contrast of a display panel can be improved. However, conventional TFTs devices employing a single layer SiO_2 or Si_3N_4 deposed by PECVD as gate insulator suffer from high interface trap density, low breakage field, high gate leakage current, and weak device reliability. These drawbacks limit the applications of LTPS TFTs. Therefore, multilayer of high-quality low-temperature gate dielectrics was proposed to overcome the foregoing problems.

In this work, low temperature poly-Si (LTPS) TFTs with sequential lateral solidification (SLS) laser annealing process was fabricated [1]. The grain boundary (GB) location can be well-controlled and fabricated in the channel of device to improve hot-carrier effect. TFTs with oxide-nitride-oxide (ONO) stacked gate dielectric were also investigated to improve device reliability. The performance between ONO stacked gate dielectric devices and conventional SiO_2 devices have been measured and analyzed under AC stress conditions. A MONOS (metal-oxide-nitride-oxide-polysilicon) memory device characteristics are also investigated.

2. Sample structure

Fig.1. shows schematic cross section of LTPS TFTs device with ONO film structure. The SEM image of SLS poly-Si grain was shown in Fig.2. The device parameters of our samples, stress and operation conditions are listed in Table 1.

3. Device Reliability of LTPS-TFT

Fig.3 and Fig.4 show the I_d-V_g characteristics shifting with stress for TFT with SiO_2 and ONO as the gate dielectric layer, respectively. The normalized shift of threshold voltage, V_{th}, on-state current, I_{on} and maximum transconductance, $G_{m,max}$, under stress of this two devices are summarized in Fig.5&6, respectively. These results show that the V_{th}, and subthreshold swing, S, increase with stress time. Especially for SiO_2-TFT device, the threshold voltage significantly increases about 4 times than initial device after 5000 seconds stress. These results suggest that the degradation is caused by electron trap charge in the gate oxide and the increase interface state density at the grain boundary [2]. The SiO_2-TFT suffers much worse stress-induced degradation than ONO-TFT device.

Under hot-carrier stress, both the devices show very limited degradation. As demonstrated in Fig.7&8, the ONO-TFTs exhibit higher immunity to hot-carrier stress than SiO_2-TFT still. From the above observations, we found a stack gate dielectric layer, ONO, can provide much better reliability for a TFT device at a dielectric EOT of 60nm. This can be due the self-blocking effect of an ONO structure as trap charge already exist in the SiN layer.

4. MONOS Memory Device Characteristics

This ONO-TFT structure can also be viewed as a non-volatile MONOS device, which can be programmed and eased by FN current. The program/erase (P/E) characteristic for MONOS memory device is shown in Fig.10. The V_{th} window about 4V after 1 sec P/E duration is demonstrated. Fig.11. shows the I_d-V_g characteristic of the device at state "0" and "1", respectively. Retention characteristic after 10^3 P/E cycle was shown in Fig.11. It exhibits good charge retention capability. Hence, this TFTs device with ONO gate structure as a 1 bit/1 cell memory device is promising.

By optimal the ONO structure, the operation voltage, program /erase speed, endurance, and data retention characteristics is expected to be further improved. Therefore, this MONOS memory device on glass is a promising candidate for non-volatile memory implementation in TFT: LCD. This work shows that the ONO-TFT structure can be integrated into the pixel array of LTPS Thin Film Transistor-Liquid Crystal Display (TFT-LCD), to reduce power consumption of LCD for mobile applications [3-7].

5. Conclusion

Sequential lateral solidified LTPS TFTs with ONO stacked gate dielectric was fabricated. This device exhibit better reliability characteristics than conventional TFTs. Furthermore, a MONOS memory device on the glass has been preliminary evaluated. These experimental results strongly support the application of ONO film structure in realizing high performance, high reliability LTPS TFTs and possible non-volatile memories.

Acknowledgements

The author would like to acknowledgement Dr. Sheng-Huei Dai and Dr. Ling-Chang Hu for helpful discussions and suggestions

Reference

[1] HT. Chen, et al., IDMC'05 (2005) 55
[2] F. V. Farmakis, et al., IEEE Elec. Dev. Let., vol.22, NO.2, February (2001) 74
[3] H. Kimura, et al., SID 01 DIGEST (2001) 68
[4] H. Tokioka, et al., SID 01 DIGEST (2001) 280
[5] M. Senda, et al., SID 02 DIGEST (2002) 790
[6] K. Yoneda, et al., VLSI Tech. Symposium (2001)
[7] Y. Nakajima, et al., SID 04 DIGEST (2004) 864

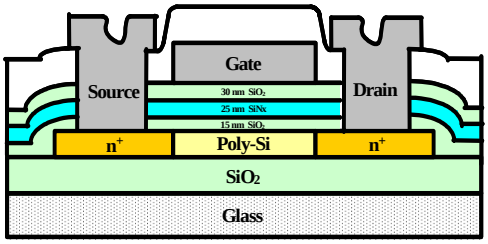

Fig.1. Schematic cross section of LTPS-TFTs device

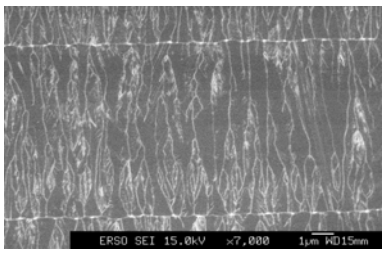

Fig.2. SEM image of SLS poly-Si grain

	V_g	V_d	V_s	
AC High-field stress	E_{eq}= 4 MV/cm	0 V	0 V	f = 50 KHz
AC Hot carrier stress	12 V	12 V	0 V	f = 50 KHz
Program	40 V	0 V	0 V	
Erase	- 40 V	10 V	10 V	
V_{th}	@ $I_d = (W/L) \times 10^{-8}$ A			
I_{on}	@ V_g = 10 V, V_d = 0.1 V			

Table 1. Stress and operation conditions

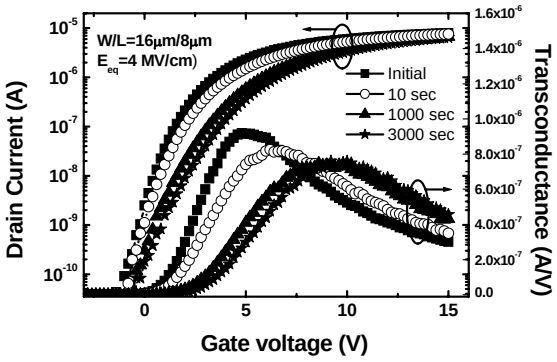

Fig.3. I_d-V_g transfer characteristic of a SiO_2-TFT before and after high-field stress (E_{eq}=4 MV/cm)

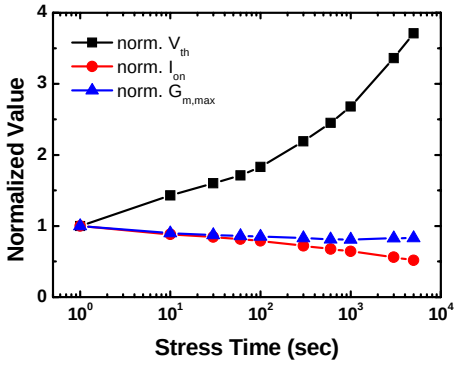

Fig.5. V_{th}, I_{on} and $G_{m,max}$ degradation as a function of stress time for SiO_2-TFT

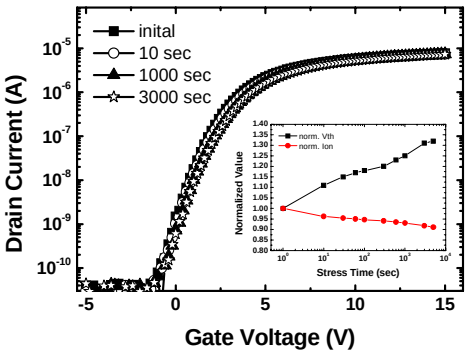

Fig.7. I_d-V_g transfer characteristic of a SiO_2-TFT before and after hot carrier stress

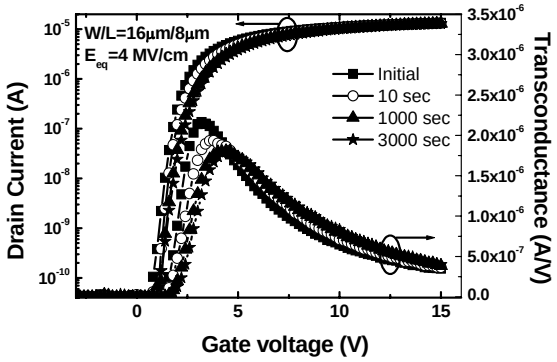

Fig.4. I_d-V_g transfer characteristic of a ONO-TFT before and after high-field stress (E_{eq}=4 MV/cm)

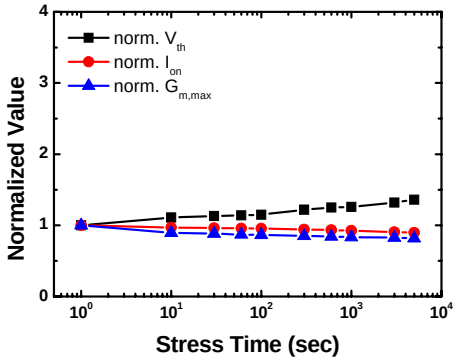

Fig.6. V_{th}, I_{on} and $G_{m,max}$ degradation as a function of stress time for ONO-TFT

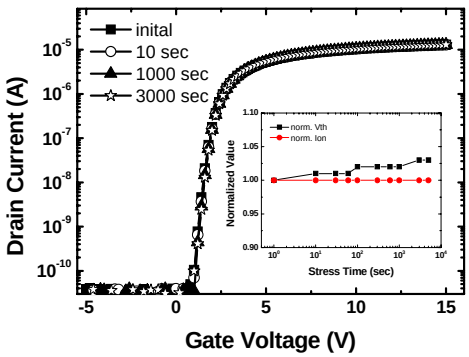

Fig.8. I_d-V_g transfer characteristic of a ONO-TFT before and after hot carrier stress

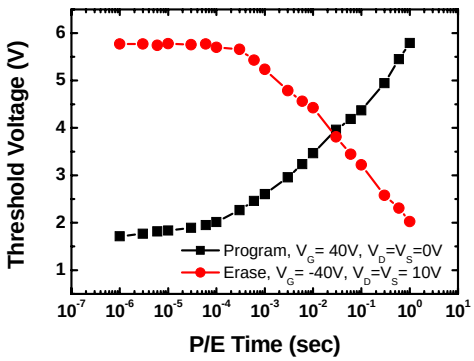

Fig.9.Program/Erase characteristics of MONOS memory device

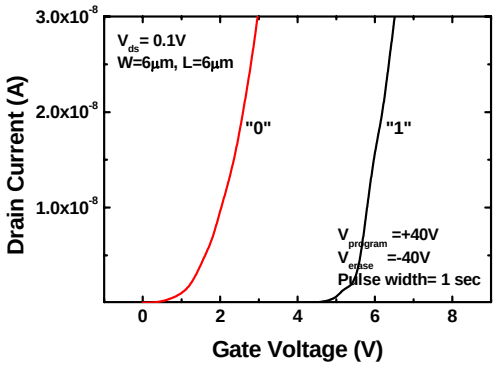

Fig.10. I_d-V_g characteristic at state "0" and "1" for a reference current

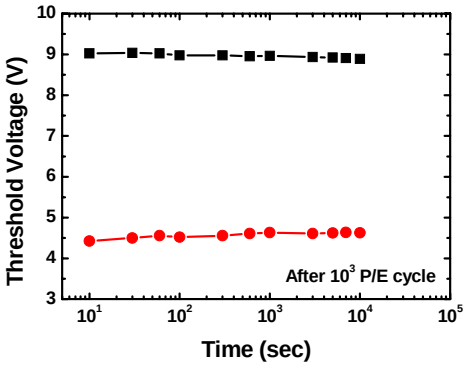

Fig.11. Data retention characteristic of MONOS memory device after 10^3 P/E cycle