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Direct measurement of the offset spacer effect on the carrier profiles in sub-50 nm p-MOSFETs

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1. Introduction

To obtain small and highly powerful devices, it is very important to optimize the design of two-dimensional (2-D) carrier profiles of source/drain and extension (SDE) and channel regions in scaled metal oxide semiconductor field-effect transistors (MOSFETs). The 2-D carrier profile is predominantly determined by thermal budget, ion implantations and their mask structures. For example, offset spacers are often used to control the lateral doping profile of extension and pocket implants. In addition to the thickness of the offset spacers, their bottom shapes are very important to determine the doping profiles. However, the effect of the bottom shape in the offset spacer on the 2-D carrier profile has not been directly measured in details. The tail-shaped bottom of the offset spacer might strongly affect the doping profile for the shallow extension region (Fig. 1(c)). In contrast, the notch-shaped bottom would mainly affect the pocket profile implanted with a high tilt angle (Fig. 1(d)). In this study, we will report the 2-D carrier profiles of the sub-50 nm p-MOSFETs with slightly different offset spacers. The 2-D carrier profiles will be directly measured by using scanning tunneling microscopy (STM) [1-3]. The origin of the difference in the electrical characteristics of the corresponding devices will be discussed from the carrier profiles.

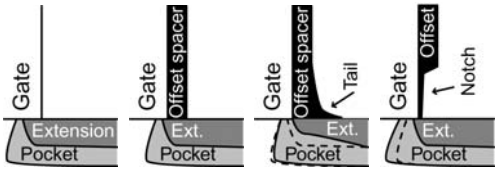

Fig. 1 Schematic illustration of the effect of the offset spacers on the doping profiles around the SDE regions (a): No offset, (b): Ideal offset, (c): Tail-shaped offset, (d): Notch-shaped offset.

2. Electrical characteristics of sub-50 nm p-MOSFETs

Two p-MOSFET samples were fabricated under a standard process for planar CMOS devices with sidewall-notches [4]. For all the samples, the process conditions except the sidewall-notch were kept constant. The bottom region of the sidewall-notch in sample B was etched more additionally than that in sample A. The key part of the fabrication process is briefly described as follows. The length of the poly-Si gate (L_{poly}) was designed to be 45 nm. After fabrication of the sidewall-notch, Sb pocket was implanted with a high angle tilt. The extension region was formed by B ion implantation at a sub-keV energy [5]. The implanted impurities were sufficiently activated by rapid thermal annealing.

Figure 2 shows Vg-Id characteristics of the 45 nm p-MOSFETs with sidewall-notch structure corresponding to *sample A* and *B*, respectively. It was found that the threshold voltage of *sample B* was lower than that of *sample A*. Based on this result, it could have been simply speculated that the effective channel length of *sample B* would have been shorter than that of *sample A*. However, the dependence of the electrical characteristics on the back bias voltage was more enhanced in *sample B* than in *sample A*, as shown in Fig. 3. This result denies the speculation mentioned above. Therefore, direct measurement of the 2-D carrier profile was required to confirm the origin.

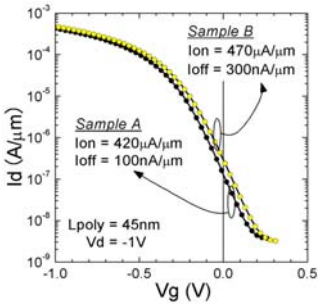

Fig. 2 Vg-Id characteristics of the 45 nm p-MOSFETs with sidewall-notch structure corresponding to *sample A* and *B*

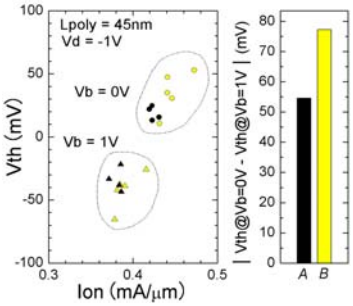

Fig. 3 Dependence of the Ion-Vth characteristics of the 45 nm p-MOSFETs on the substrate bias voltage

3. 2-D carrier profiles in sub-50 nm p-MOSFETs

After H-terminated cross-sectional planes of the p-MOSFET samples were prepared, 2-D carrier profiles were measured by using STM [3]. Figure 4 shows the 2-D

carrier profiles of the sub-50 nm p-MOSFETs. The geometric outline of the p-MOSFETs including silicon recesses can be observed as a topographic STM image. For simplification, the following STM current images (carrier profiles) are indicated with the schematic outlines obtained from the topographic images. The vertical junction depth (X_j) and the lateral overlap length (X_{ov}) of the extension regions are defined as shown in Fig. 4(a). The lateral overlap length is estimated at a depth of 5 nm. Figures 4(b) and 4(c) show the 2-D carrier profiles around the SDE and channel regions in *sample A* and *sample B*, respectively. It was found that the vertical junction depth was almost the same between both samples. In contrast, it was found that the lateral overlap length of *sample A* was longer than that of *sample B*. For quantitative comparison, the average value of each parameter was estimated from the results measured for a number of transistors, as summarized in Table 1. The average Xov of *sample A* was longer by 2 nm than that of *sample B*. Moreover, the lateral abruptness of the extension region at a depth of 5 nm in *sample B* was steeper by 25 % than that in *sample A*, as shown in Fig. 5. It is considered that doping profile of the Sb pocket implant mainly caused such a variation of the carrier distribution. The peak position of the Sb pocket near the lateral junction in *sample B* was deeper than that in *sample A* because the slightly upped bottom of the sidewall-notch (< 5nm) reduced the screening distance for the Sb pocket implant as shown in Fig. 6. Based on this model, it is considered that the top channel concentration near the lateral junction decreased in *sample B*. The measured carrier profiles suggest that the drive current increases together with lowering a threshold voltage for the p-MOSFET of *sample B*. The variation in the electrical characteristics expected from the carrier profiles is consistent with the measured results mentioned above. Therefore, the 2-D carrier profiling technique had confirmed the origin of the offset spacer effect on the electrical characteristics.

4. Conclusions

We have directly measured the effect of the bottom shape in the offset spacer on the 2-D carrier profiles of the sub-50 nm p-MOSFETs. It has been found that the doping profile of the Sb pocket implanted with a high angle tilt is very sensitive to the bottom shape of the notched offset spacers. It has been confirmed that the Sb pocket deeply implanted leads to the decrease of 2 nm in the average overlap length of the extension region when the bottom is slightly upped at the notched offset spacer. Moreover, the reduction of the carrier concentration in the top channel region lowers the threshold voltage and enhances its dependence on the back bias voltage. Therefore, the 2-D carrier profiling techniques can confirm the unexpected origin of variation in the electrical characteristics.

References

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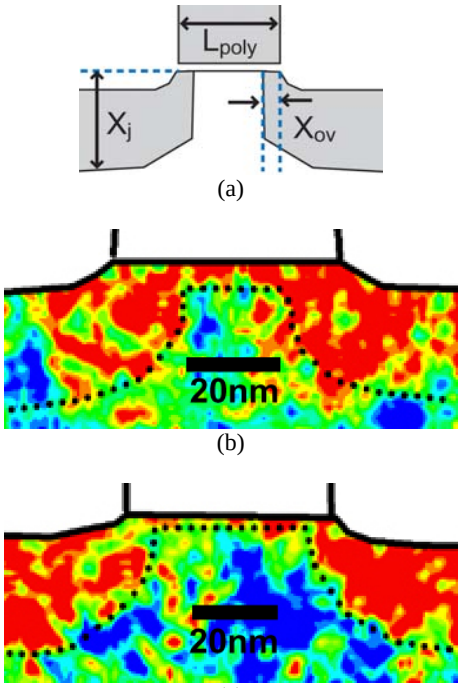

Fig. 4 Carrier profiles in the sub-50 nm p-MOSFETs
(a): Schematic illustration of the definition of the parameter.
(b): *Sample A*. L_{poly}= 48 nm, X_{ov}= 12 and 13 nm.
(c): *Sample B*. L_{poly}= 48 nm, X_{ov}= 6 and 7 nm.

Table 1. Summary of the measured parameter

	L_{poly}	σL_{poly}	X_j	σX_j	X_{ov}	σX_{ov}
Sample A	46	2	28	1	10	2
Sample B	47	2	29	1	8	2

[All units: nm]

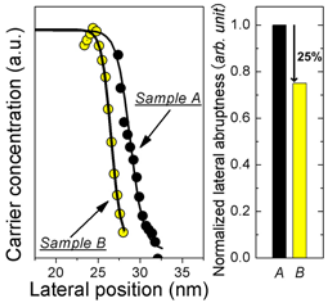

Fig. 5 Comparison of the lateral carrier profiles across the extension regions between *sample A* and *B*

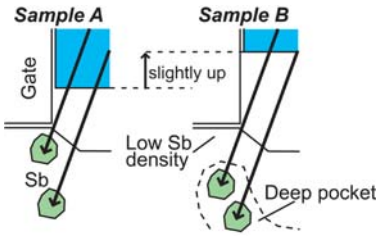

Fig. 6 Schematic illustration of the origin of the difference in the carrier profile between *sample A* and *B*