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Degradation of Current Drivability of Schottky Source/Drain Transistors with High-k Gate Dielectrics and Possible Measures to Suppress the Phenomenon

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Abstract
In this paper it is shown that current drivability is significantly degraded in the case that high-k gate dielectrics are adopted in Schottky source/drain transistors. This phenomenon can be understood in terms of fringing-induced barrier shielding (FIBS). Some structures are studied from the viewpoint of improvement in current drivability of Schottky source/drain transistors with high-k gate dielectrics.

1. Introduction
The trend toward miniaturization has resulted in thinning of gate dielectrics and lowering of source/drain resistances, and according to the ITRS, they should be less than 1 nm and 150 Ωμm, respectively, within 5 years. In order to avoid the drastic leakage current increase that is inherent in such thin SiO_2 gate dielectrics and to reduce source/drain resistances, high-k materials for gate dielectrics and Schottky source/drain transistors (STR) are being intensively investigated [1, 2]. In this report, we quantitatively investigated current drivability of STR with high-k gate dielectric and found that it is significantly degraded. Thorough investigations of the structure dependence of the phenomena indicated that the degradation mechanism resides in FIBS [3]. Some structures for the improvement of the current drivability of STR with high-k gate dielectrics are also shown.

2. Model in Simulation
Electrical characteristics were simulated for 35 nm channel length nMISFETs having metallic sources and drains at 300K (Fig. 1). We used an in-house 2-dimensional device simulator (DIAMOND), taking both thermal and tunneling current through Schottky junctions and barrier height lowering due to image charge into consideration. The impurity concentration in the substrate was $1x10^{16}$ cm^{-3} at the substrate surface and $1x10^{18}$ cm^{-3} deep inside. The equivalent oxide thickness (EOT) of gate dielectric was set to be 1 nm. Gate electrode was aluminum. Xj of the source/drain metal was set to be 10 nm and the Schottky barrier height of the material was assumed to be as low as 0.2 eV. Passivation layer was assumed to be SiO_2. V_{TH} adjustment was not carried out in this study.

3. Results and Discussion
3.1. Current Drivability of High-k STR
Fig. 2 shows that current drivability of STR with high-k gate dielectric is seriously degraded and that this tendency becomes more significant as a dielectric constant of gate dielectrics increases. The degradation is more serious than that of conventional MISFETs, the amount of which is only 25% even in the case of k = 200 [3]. Fig. 3 shows that current drivability is degraded also in the case that gate and source/drain have an offset. In order to clarify the reason for the degradation, the electrical potential around the source region was examined. Fig. 4 shows that electrical potential in channel region is lower, i.e., Schottky barrier is thicker, in high-k gate dielectric devices than in low-k gate dielectric devices, resulting in the degradation of current drivability. This phenomenon can be understood in terms of FIBS [3], which means that electrical potential at channel surface is influenced by capacitive coupling between channel and source due to lines of electric force through high-k gate dielectrics resulting in a thickening of Schottky barriers. FIBS can also explain the tendency in Fig. 3 in the case of the device with an overlap. The degradation in the case of the device with an offset can be understood in terms of weakening of the capacitive coupling between gate and channel region near source, resulting in thickening of Schottky barriers as shown in Fig. 5.

3.2. STR with Stacked Gate Dielectrics
In order to study effects of low-k interfacial layers on FIBS, current drivability of devices with stacked gate dielectric structures (Fig. 6) were simulated. Fig. 7 shows that although current drivability of devices with an offset is degraded, interfacial layers effectively suppress current degradation of devices with an overlap due to FIBS. This is because low-k interfacial layers reduce the capacitive coupling between source and channel. In some cases, simulations did not converge. In order to study influences of interfacial layers on off-state characteristics, V_{TH}(=V_G @I_D = 0.1 μA/μm) was calculated. Fig. 8 shows that the influences are quite small. Hence, low-k interfacial layers at high-k layer/substrate interfaces are quite effective for suppressing current degradation due to FIBS without influencing off-state characteristics.

3.3. STR with High-k Sidewalls
When source/drain of STR is fabricated by silicidation technique, gate sidewalls are quite effective for avoiding the "bridging phenomenon." However, they make it quite difficult to realize source/drain with shallow x_j without offsets between gate and source/drain. In order to suppress the degradation of current drivability due to offsets, structures having gate sidewalls with high dielectric constant (Fig. 9) are proposed. Fig. 10 shows that there is an optimum, which is at an offset length of about 2 nm. The reason for the existence of an optimum can be understood in terms of a tradeoff between a decrease in capacitive coupling between gate and channel in the case of offsets and an increase in capacitive coupling between source and channel, i.e., FIBS, in the case of overlaps. In some cases, simulations did not converge. It should be noted that EOT between gate and substrate in the gate sidewalls is thinner than 1 nm. However, this "thinner EOT" alone cannot explain the high current drivability because current drivability depends on the order of stacking in the stacked gate dielectrics (Fig. 11). In order to study the reason for the increase in current drivability, potential profile near source edge was simulated. Fig. 12 shows that lines of electric force have corners at the side surface of the interfacial layer due to refraction at the interface between two materials with different dielectric constants, and that they are concentrated on source edge, i.e., capacitive coupling between gate and channel is enhanced. This is a reason for the increase in current drivability. In order to estimate the amount of the effect of the refraction, difference of drain current between 2 cases shown in Fig. 11 (= ΔI_D) was studied, which is considered to give a lower bound of the effect. Fig. 13 shows that more than 10% of I_D is due to the effect of refraction. Also in this case, influences of the structure on off-state characteristics are quite small. Hence, high-k gate sidewalls and stacked gate dielectrics are quite effective for increasing current

drivability without influencing off-state characteristics.

4. Summary and Conclusion

It has been shown that current drivability of Schottky source/drain transistors with high-k gate dielectrics is significantly degraded. Designing device structure using refraction of lines of electric force can improve current drivability of devices with high-k gate dielectrics.

References

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[2] M. P. Lepselter, et al., Proc, IEEE **56** p.1088 (1968)
[3] D. L. Kencke, et al., DRC Tech. Dig. p.22 (1999)

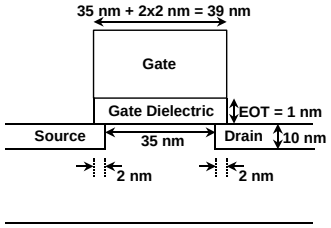

Fig. 1. Device structure used in the simulation.

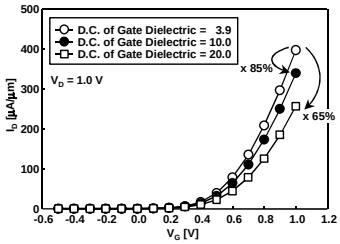

Fig. 2. I_D-V_G characteristics of devices with gate dielectrics of various dielectric constants (D.C.).

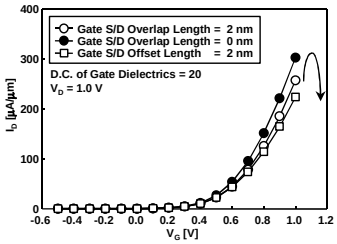

Fig. 3. I_D-V_G characteristics of devices with various overlap/offset lengths between gate and source/drain.

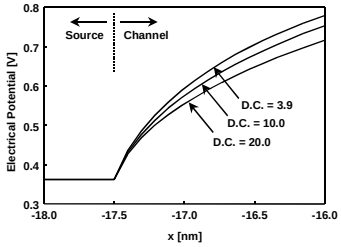

Fig. 4. Electrical potentials at the substrate surface near the source/channel interface in devices shown in Fig. 2 at $V_G = V_D = 1.0$ V.

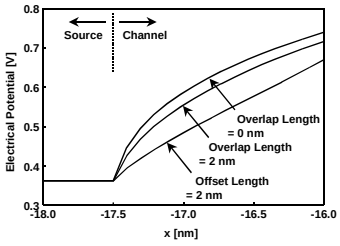

Fig. 5. Electrical potentials at the substrate surface near the source/channel interface in devices shown in Fig. 3 at $V_G = V_D = 1.0$ V.

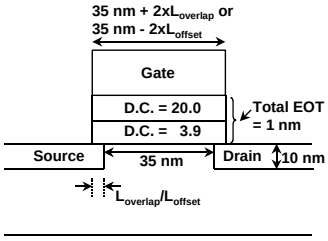

Fig. 6. Stacked gate dielectric structure used in the simulation.

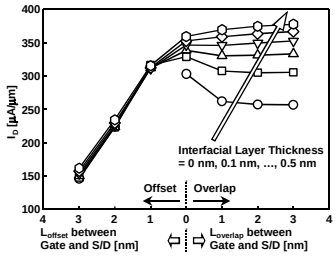

Fig. 7. Dependences of I_D($V_G = V_D$ = 1.0 V) on overlap/offset length between gate and source/drain.

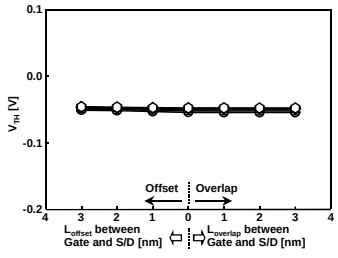

Fig. 8. Dependences of V_{TH}(= V_G @I_D = 0.1 μA/μm) on overlap/offset length between gate and source/drain.

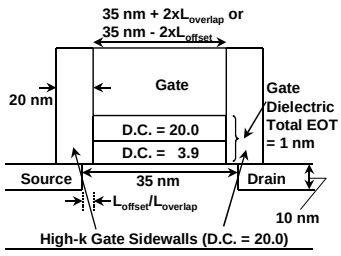

Fig. 9. Structure used in the simulation with high-k gate sidewalls.

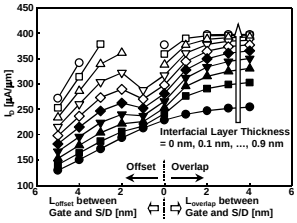

Fig. 10. Dependences of I_D($V_G = V_D$ = 1.0 V) on overlap/offset length between gate and source/drain.

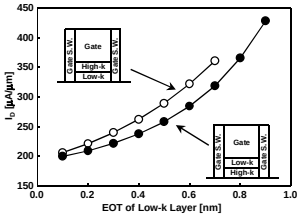

Fig. 11. Dependences of I_D($V_G = V_D$ = 1.0 V) on EOT of low-k layer in the device with high-k gate sidewalls and an offset length of 2 nm.

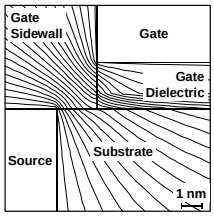

Fig. 12. Equipotential curves near source edge in a device with an interfacial layer thickness of 0.7 nm and an offset length of 2 nm at $V_G = V_D = 1.0$ V.

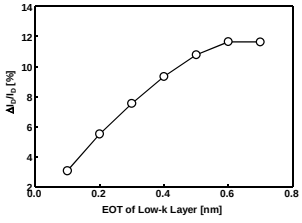

Fig. 13. Dependence of a ratio of ΔI_D to I_D at $V_D = V_G$ = 1.0 V on EOT of low-k layer in the device shown in Fig. 9 with an offset length of 2 nm.