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Cu/low-k process integration for 65nm and 45nm SoC devices

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Introduction

Demands for continued down scaling and performance improvement of the wiring system arise in every generation. Therefore, a robust interconnect technology that gives both an accurate damascene etching profile control and sufficient reliability is indispensable for copper interconnects with lower k-value material. We have applied a hybrid scheme since 65nm technology node to meet these requirements. Excellent dual damascene (DD) profile could be obtained with porous low-k materials due to high etching selectivity of PAr/SiOC. Furthermore, the hybrid scheme made replacement with the lower-k materials easy so that development of 65nm technology was able to be shifted to the development of 45nm technology smoothly. Although a technology hurdle of the dual damascene formation could be lowered by using the hybrid scheme, there were still some issues to be solved in the 45nm node such as poor mechanical integrity, film property degradation due to plasma process induced damage and reliability. In this paper, the hybrid scheme applied since 65nm node and critical points of newly developed 45nm BEOL technology are discussed.

Hybrid scheme of PAr/SiOC integration

Homogeneous SiOC inter layer dielectrics (ILD) structure with via-first process has been widely developed since 90nm node. We have also applied the process in the 90nm node [1]. However, as shown in Table 1, we have changed the ILD scheme to the hybrid (PAr/SiOC) from the 65nm technology to balance the requirements of reliability and the demand for down scaling and high performance [2-3]. Figure 1 shows the cross-sectional TEM image of 2-level module developed for 45nm node applying the hybrid scheme. A precise DD profile control of porous low-k film is realized. The hybrid scheme is not only superior to the profile controllability, but also relatively insensitive to the mechanical integrity due to smaller volume of the fragile porous-SiOC and a stress relaxing effect by tough organic film [4-5]. This means that we can focus on the development of damage resistant porous low-k films when choosing the hybrid scheme.

Damage and moisture control for porous low-k integration

As long as we choose the hybrid scheme, it is relatively easy to extend the 65nm to the 45nm BEOL technology, replacing the ULK film with the porous low-k film. It was relatively easy to obtain a high pass yield in large-scale normal via-chains and in wiring-open/-short as shown in Figs. 2 and 3, respectively. However, the most difficult and important issue to be solved in the porous low-k integration is suppression of the degradation of via characteristics and reliability degradation, which are caused by moisture from porous ILD films as shown in Fig. 4. In developing highly reliable 45nm BEOL integration, we focused on the following items:

(1) Damage Reduction for porous low-k dielectrics

1-1 Development of damage resistant low-k material;

Development of a damage resistant ILD film should be the first priority in the development of porous low-k integration. Particularly, damage resistance of the ILD used for via layer is the most important requirement [6]. The best porous SiOC film was selected from among many candidates and the film quality was improved to reduce the plasma damage which has great impact on SiV (stress induced voiding) failures [5].

1-2 Insertion and improvement of low-k buffer layer;

A low-k (k=3.0) buffer layer was inserted for porous SiOC film to suppress the damage during trench etching process [6]. To obtain the maximum protection effect of the buffer layer, a damage resistant buffer film was newly developed as well as porous low-k films. By inserting the improved buffer layer, carbon depletion is drastically reduced as shown in Fig.5.

(2) Metallization

We focused on the development of a metallization technology for controlling moisture uptake, oxidation induced volume expansion and morphology degradation of barrier metal for 45nm porous low-k integration. Figure 6 shows yields of Kelvin (sparse) vias. There was no difference in the resistance distribution between conventional and developed metallization technology when a dense low-k (k=2.65) CVD-SiOC film was used as a via-ILD film. However, when a porous low-k film was applied as the via-ILD film, significant yield degradation was observed in conventional metallization process. Therefore, a newly developed metallization process for controlling moisture uptake, oxidation and morphology of barrier metal is indispensable in the porous low-k integration.

(3) Wiring dummy pattern

The most effective measure for reliable Cu interconnects with porous low-k ILD is the control of the wiring coverage by adding a dummy wiring pattern. By the opening of a dummy wiring pattern, moisture in porous SiOC film is efficiently removed. As shown in Fig. 7, the pattern dependence problem was solved by adoption of a dummy pattern. Moreover, the difference of the damage resistance between low-k films is also canceled by setting the dummy wiring pattern. Introduction of the dummy pattern optimized from the viewpoint of not only controlling the process variation attributable to CMP, but also of improving reliability is indispensable for robust and reliable porous low-k integration for the 45nm technology node and beyond.

Reliability

Porous low-k integration providing practical wiring performance and reliability was realized by introducing the above-mentioned technologies to control damage and moisture. Figure 8 shows the result of stress-migration reliability test for the developed 45nm double-level Cu dual damascene interconnects (via size=75nm). A drastic SiV-reliability improvement was obtained in SiV-TEG with wide upper metal wiring, which is sensitive to SiV mode failures. Furthermore, EM test results with over 1.5 orders improvement and sufficient TDDB lifetime have been obtained.

Conclusions

The hybrid ILD (PAr/SiOC) scheme was developed and applied to the 65/45nm BEOL technologies to meet the requirements concerning scaling and realization of a high-performance interconnect system with sufficient reliability. A highly reliable BEOL technology with porous low-k film (k=2.3) was developed for 45 nm (hp65) node high-performance devices. The moisture control techniques for a low-k film were intensively developed. By introducing technologies such as damage resistant porous PAr/SiOC materials, damage resistant low-k buffer film, a developed metallization technology for oxidation control and wiring pattern coverage control by means of dummy pattern, the porous low-k (k=2.3) integration satisfying practical reliability was realized.

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References

[1] K.Higashi et al., Proc. of IITC (2002), pp15-17.
[2] R.Kanamura, et al., Symp. on VLSI Tech. (2003), pp107-108.
[3] A.Kajita et al., Proc. of IITC (2003), pp9-11.
[4] H. Kitsutaka et al., Proc. of AMC (2004), pp265-268
[5] H.Miyajima et al., IEDM Tech. Dig. (2004), pp329-332
[6] N.Nakamura et al., Proc. of IITC (2004), pp228-230.

Table 1 BEOL structures for 90, 65 and 45nm technology node

Node	90nm	65nm	45nm
Structure	Homogeneous	Hybrid	Hybrid
Cap	SiO_2 (k=4.1)	SiO_2 (k=4.1)	SiOC (k=3.0)
Trench	SiOC (k=2.9)	PAr (k=2.65)	Porous PAr (k=2.3)
Via		SiOC (k=2.5)	Porous SiOC (k=2.3)
Barrier	SiCN (k=4.9)	SiC (k=3.5)	SiC (k=3.5)
keff	3.3	3.0	2.7

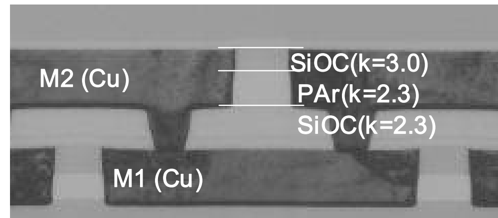

Fig.1 Cross-sectional TEM image of 2-level intermediate module with porous low-k (k=2.3) films.

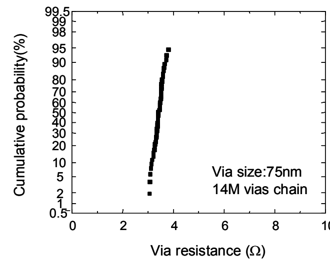

Fig.2 Via resistance distribution of large-scale (14M vias) via chain with porous low-k (PAr/SiOC, k=2.3) material.

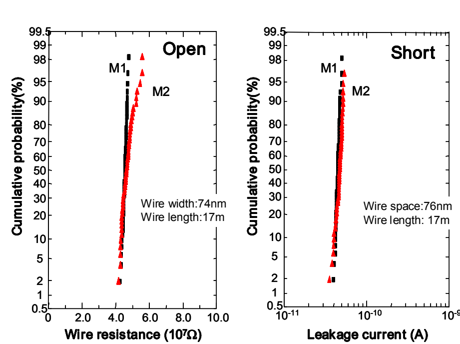

Fig.3 Cumulative distribution for resistance of 17m wiring (left) and wire-to-wire leakage current (right)

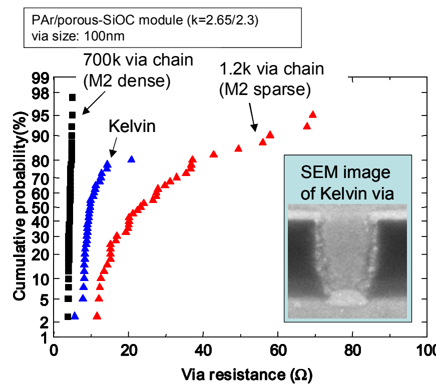

Fig.4 Pattern dependence of via chain failures due to barrier metal oxidation.

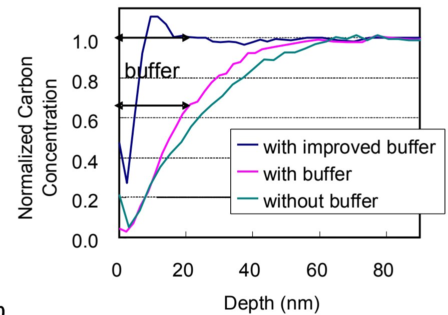

Fig.5 Carbon profile in the buffer/porous-SiOC films after RIE damage.

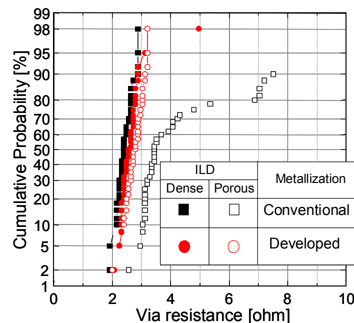

Fig.6 Cumulative resistance distribution of Kelvin via pattern. Advantage of the developed metallization becomes clear for porous low-k film.

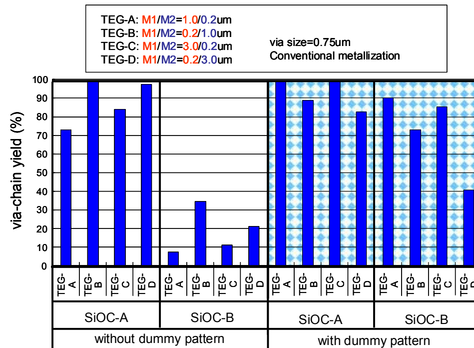

Fig.7 Dummy pattern impact for reduction of pattern/ILD material dependence of via failures.

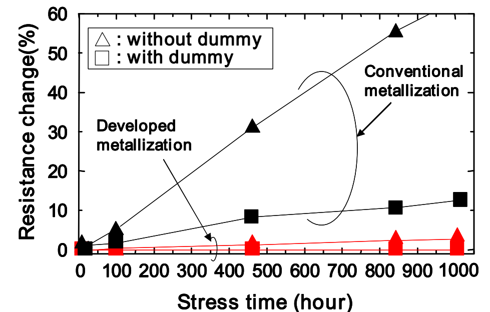

Fig. 8 Resistance change in SiV sensitive via chain (M2 W=1.0 μm, via size =75 nm) pattern during SM test (Temp. =175C).