Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.918-919

C-10-2

Realization of A Metal Split Gate By Gate Full Ni-Silicidation Process For MOSFET RF/Analog Applications

Jun Yuan, Jason C. S. Woo
Electrical Engineering Department, University of California, Los Angeles, CA, USA, 90095
Email: Jun_yuan@ee.ucla.edu Woo@ee.ucla.edu

1. Introduction

High-performance CMOS system-on-chip (SOC) design requires RF MOSFETs integrated with digital circuits. However, MOSFET design optimized for digital applications often results in a degraded RF/analog performance, such as intrinsic gain (g_m*r_{out}). A novel split gate design shown in Fig.1 was proposed to obtain high-frequency characteristics with good gain performances [1], i.e, having both high transconductance (g_m) and output resistance (r_{out}). However, the split gate device can be utilized only if its fabrication process is compatible with that of conventional gate devices. Long et. al. [2] demonstrated a similar gate structure by using tilt angle evaporation of two different metals on the gate of a InGaP/InGaAs HFET. But this method is difficult to implement in conventional CMOS processing. Hence, unique process technologies compatible with the CMOS process are needed to realize this split gate structure. In this work, the fabrication of split gate MOSFETs was realized by full nickel-silicidation of the polysilicon gate combined with NiSi gate work function tuning at the drain side through tilt angle implantations. Metal gate advantages and NiSi process simplicity were realized in the split gate process.

2. The proposed split gate HL MOSFET structure

Fig.1(a) shows the 2-D structure of a split gate HL device. The gate electrode is laterally composed of two electrodes with different work functions (H: high work function; L: low work function). The work function difference between the H and L gate electrodes causes an abrupt change in the conduction band energy at the silicon surface. This generates an electric field peak in the channel with a high electric field slope at the source side (Fig.1(b) & inset). Hence, source carrier injection into the channel is enhanced and g_m is improved [1]. Furthermore, the HL gate device has high inversion charge density under the L gate due to its lower work function. Hence, less channel-length-modulation is expected in the HL split gate device, subsequently leading to a higher r_{out}[3].

3. Process design

Full nickel-silicidation of the polysilicon gate is a promising metal gate technology. It was reported [4,5] that the NiSi gate work function can be modified due to dopant segregation effects at the oxide interface. Fig.2(a)(b) shows that antimony (Sb) implanted in the poly gate reduces the NiSi work function after the gate full-silicidation process. If the Sb dopants can be segregated locally in a NiSi gate (at the drain side), this forms a NiSi HL split gate -- the work function is lower for the NiSi gate with Sb dopants under it, which is close to the drain side.

The process flow diagram is shown in Fig.3. First, Gate stack of oxide/polysilicon/LTO was formed, and the LTO was patterned by the gate lithography. Antimony was implanted into the gate polysilicon from the drain side with a tilt angle (Fig.3(a)). Polysilicon was only patterned after the gate implantation to prevent the source/drain (S/D) regions from being simultaneously doped. After the polysilicon gate definition using the LTO as a hard mask, nitride spacer was formed. The LTO dummy gate which increases the gate stack height during the nitride spacer formation (Fig.3(b)), was removed by a BOE solution (Fig.3(c)). Finally, a nickel film was sputtered and silicidation was performed on the polysilicon gate and the S/D regions by a 10 minute anneal at 450 ^{o}C (Fig.3(d)).

4. Characterizations of MOSFETs with NiSi split gate

Fig.4(a) shows that the nitride spacer was not attacked by the BOE solution during the removal of the LTO stack. After the nickel silicidation process, it can be seen that the gate was fully silicided, and at the same time the S/D regions were also silicided as shown in Fig.4(b). The nitride spacer serves as an isolation between the gate and the S/D regions after silicidation.

Capacitance-voltage characteristics for an undoped NiSi gate and a n-type poly gate capacitor (100μm x 100 μm) are shown in Fig.5(a). No poly depletion effect was observed in the NiSi gate. Furthermore, the threshold voltage of the fully-silicided gate confirmed the mid-gap work function of NiSi [5]. The low gate leakage current (pA order) shown in Fig.5(b) demonstrates that the low temperature full Ni-silicidation process doesn't degrade the gate oxide quality. No short exists between the gate and the S/D after the silicidation process due to the good isolation from the tall nitride spacer.

Fig.6(a) shows the I_{ds}-V_{ds} characteristics for 0.6 μm gate length NiSi MOSFETs on undoped substrates. The MOSFET having polysilicon gate implanted with Sb from the drain side prior to the gate full silicidation process clearly demonstrates a higher current drive capability than the MOSFET with an undoped NiSi gate. This indicates that the tilt-angle implanted Sb in the polysilicon gate was segregated locally in the gate after the nickel silicidation process, thus forming a NiSi split gate with different work functions from the source side to the drain side. NiSi gate MOSFETs with/without Sb tilt angle implantations have comparable r_{out} at low bias current levels as shown in Fig.6(b). It is due to the fact that r_{out} is caused by the large DIBL as a result of undoped substrates. At high bias current levels, r_{out} is dominated by the channel-length-modulation. The MOSFET with a tilt-angle Sb-doped NiSi gate has a larger r_{out} as expected due to a less channel-length-modulation.

5. Conclusions

By implanting antimony (tilt angle) into the polysilicon gate from the drain side before the gate full silicidation process, the NiSi split gate has been achieved using dopant segregation effects. Gate oxide was not degraded after the full silicidation process, and no poly-depletion-effect was observed in the NiSi gates. Improved current drive capability and output resistance have been observed in the MOSFET with a NiSi split gate.

Reference

1. Jun Yuan, Jason C.S. Woo, SSDM, 2003, pp.436-437
2. W. Long, K. K. Chin, IEDM Tech. Dig., 1997, pp.549-552
3. J. H. Huang, et al, IEDM Tech. Dig., 1992, p. 569-572
4. J. Kedzierski, et al., IEDM Tech. Dig., 2003, pp. 13.3.1-13.3.4
5. Jun Yuan, Jason C.S. Woo, IEEE EDL, Vol.26,No.2, 2005, pp.87-89

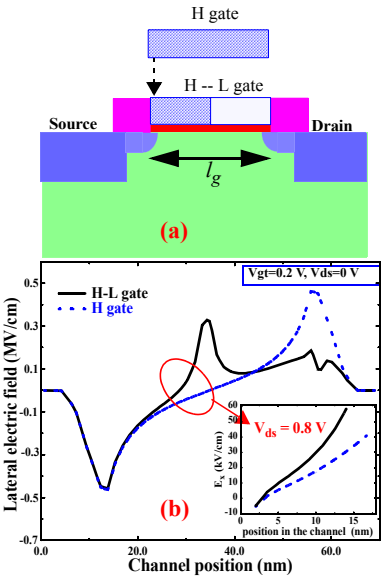

Fig.1 (a) 2-D view of a MOSFET with an HL split gate design. H: high work function; L: low work function. (b) Lateral electric fields in the channel for an H gate and an HL gate MOSFETs. Higher electric field close to the source side in the HL gate device enhances source carrier injection into the channel, thus improving g_m.

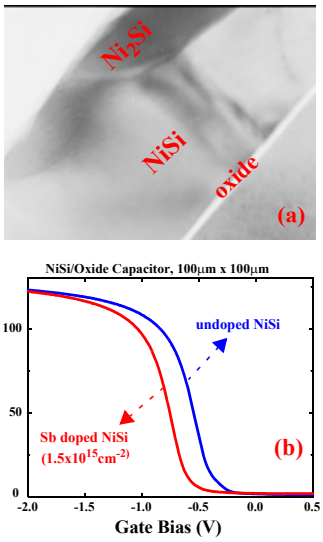

Fig.2 (a) TEM view of a fully nickel-silicided (NiSi) gate on 2.6nm oxide. (b) C-V curves for NiSi gate capacitors on 2.6nm oxide. Doping Sb in the polysilicon gate before the gate silicidation process reduces the NiSi work function.

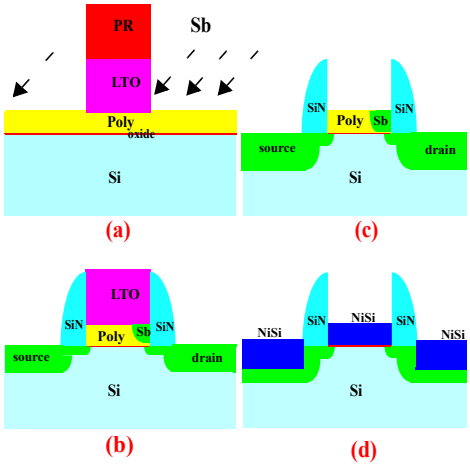

Fig.3 Process flow diagrams for NiSi split gate:
(a) Oxide(4.5nm) / Poly(50nm) / LTO(220nm) gate stack formation; LTO etch; Sb tilt-angle implant from the drain side (25KeV, 2.5x10^{15} cm^{-2}).
(b) Nitride spacer formation after the poly etch.
(c) LTO removal with BOE (20:1) solution.
(d) Nickel film deposition (~40nm) and silicidation (450 ^{o}C); Removal of the residual nickel film.

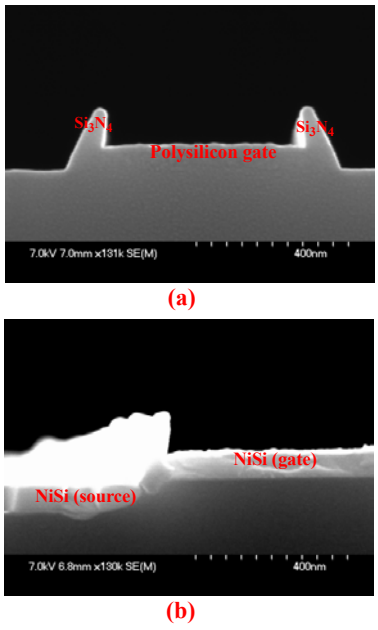

Fig.4 (a) SEM view of the gate stack after the LTO was wet etched. The unetched nitride spacer serves as an isolation between the gate and the S/D regions during the silicidation process. (b) SEM view of the gate stack after the nickel silicidation. Gate was fully silicided. The S/D regions were also silicided.

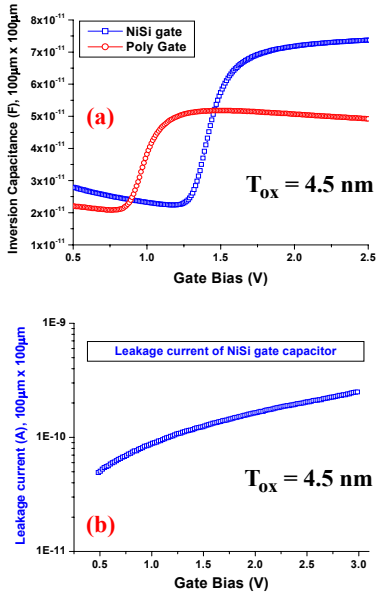

Fig.5 (a) Capacitance-Voltage characteristics of a NiSi gate and a poly gate (n-type) MOSCAPs (100μm x 100μm). No poly-depletion was observed in the NiSi metal gate. (b) Leakage current of the NiSi gate MOSCAP. No gate oxide degradation and no short between the gate and the S/D were observed after the silicidation process.

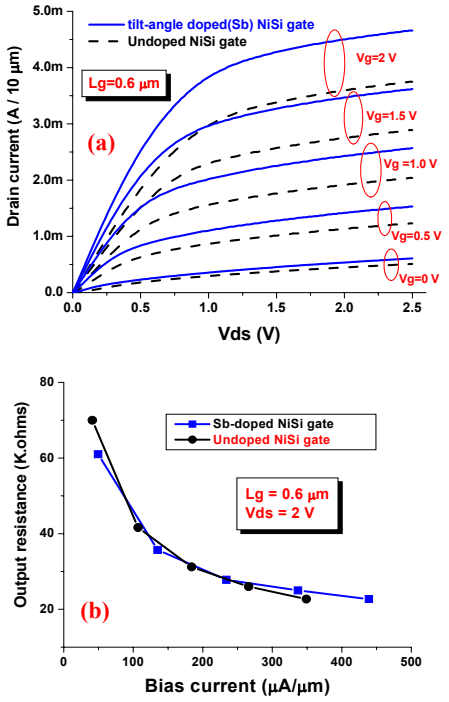

Fig.6 (a) Measured I_{ds}-V_{ds} characteristics of NiSi gate MOSFETs with 0.6 μm gate lengths and undoped substrates. The MOSFET with such Sb-doped NiSi gate (tilt-angle, 30 ^{o} from the drain side) shows an improved current drive capability. (b) Measured output resistances for NiSi gate MOSFETs w/o tilt-angle Sb implantations. Gate lengths are 0.6 μm, and substrates are undoped.