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Stress voltage polarity dependent threshold voltage shift behavior of ultrathin Hafnium oxide gated pMOSFET with TiN electrode

Hokyung Park[1,4], Rino Choi[2], Byoung Hun Lee[3], Chadwin D. Young[2], Man Chang[1], Jack C. Lee[4] and Hyunsang Hwang[1]
[1]Department of Materials Science and Engineering, Gwangju Institute of Science and Technology, #1, Oryong-dong, Buk-gu, Gwangju 500-712, KOREA
[2]SEMATECH, Austin, Texas, U. S. A., [3]IBM Assignee
[4]Advanced Materials Research Center, The University of Texas at Austin, Texas, U. S. A
Phone: +82-62-970-2314, Fax: +82-62-970-2304, e-mail: hwanghs@gist.ac.kr

Introduction:

Due to high direct tunneling current and reliability limitations of ultrathin SiO_2, high-k gate dielectrics will be used in sub-1nm technology [1]. HfO_2 and Hafnium based oxide materials are the most promising gate dielectric material for aggressively scaled device. However, studies on breakdown mechanism [2,3] and polarity dependence reliability [4,5] are still limited. In this presentation, we report on stress polarity dependent threshold voltage shift behavior of HfO_2 pMOSFETs with TiN electrode.

Experiment:

After standard cleaning, HfO_2 (3nm) and HfSiO (3nm) layers are deposited. 10nm ALD TiN layer and 100nm amorphous silicon layer were deposited as a stack electrode. After the thin nitride deposition, 90nm nitride spacer is formed and source/drain is implanted with As and B and activated using 1000°C, 10sec RTA in N_2 ambient. Finally, conventional forming gas annealing was performed at 480^{o}C for 30 minutes. To minimize an edge effect, threshold voltage shift measurement was performed with large area transistors (20μmx20μm). For charge pumping measurement, small area transistors (1μmx10μm) were used due to a leakage current limitation.

Results and discussion:

Figure 1 shows I_d-V_g characteristics under negative (inversion-gate injection) and positive (accumulation-substrate injection) stress with varying the stress time. Both positive and negative stresses showed the negative threshold voltage (V_{th}) shift. For negative stress, V_{th} shifts are parallel shifted more negatively, indicating positive charge accumulation in oxide with minimal subthreshold swing (S.S.) degradation. For positive stress, threshold voltages are also shifted negative side with severe S.S. degradation. Xu et al. reported similar behaviors in MOS capacitors with TiN/HfO_2 stack [6]. To investigate why there is no polarity dependence, transconductance (g_m) degradation during the stress is investigated (figure 2). Negative stress case showed worse g_m degradation than positive stress case and saturation of g_m degradation was slower. The distinctly different g_m degradation behaviors suggest that there might be different degradation mechanisms in different polarity stress. Figure 3 summarizes field dependent V_{th} shifts of pMOSFET 30Å HfO_2 under positive and negative constant voltage stress. Regardless stress voltage and polarity, V_{th} shifts were negative.

To find if this phenomenon is unique to HfO_2, V_{th} shift behavior of 30Å HfSiO (20% Si) pMOSFET under positive voltage stress was compared with 30Å HfO_2 pMOSFET (figure 4). Unlike HfO_2, HfSiO showed positive V_{th} shift under positive stress, indicating negative charge accumulation. Thus, stress polarity independent V_{th} shift appears to be unique to HfO_2.

To investigate this phenomenon in detail, the injection current, gate (I_g), substrate (I_{sub}) and source/drain ($I_{S/D}$) current were monitored during positive stress bias (figure 5). In HfO_2 30Å device, gate current during positive stress solely consists of electron injection from substrate, indicating that electrons injection into HfO_2 actually causes negative V_{th} shift (positively charged defects) while same electron injection in HfSiO generates a positive V_{th} shift.

It is not clear how electron generates positively charged defect status in HfO_2 layer. Thus, interface states (N_{it}) change during the stress is measured with a fixed amplitude charge pumping method at 10KHz and 1MHz to probe both interface and near interface bulk defects [7]. For negative stress, significant initial N_{it} degradation was observed in both frequencies and the recovery during relaxation cycle (0V, 10^3Sec) was relatively small (figure 6). For positive stress, N_{it} degradation at 1MHz was smaller than negative stress and the recovery of N_{it} was faster during relaxation in both frequencies. I_d-V_g characteristics change under a positive stress is shown in figure 7. After a relaxation cycle, swing is recovered to the initial value while V_{th} shift is not recovered. This result can be explained with two defect states generated by a positive stress: 1) positively charged states in bulk HfO_2 causing more persistent V_{th} shift, 2) negatively charged states at interfacial layer with short lifetime, possibly electron charging. These two mechanisms compete as a function of electric field as shown in figure 8. When a relaxation cycle after a negative bias was performed at low positive bias, the recovery was limited and saturated soon. On the other hand, at high positive bias, V_{th} was recovered close to the initial value immediately and then, positive charges were slowly built up. It means that the positive charges accumulated under negative bias can be de-trapped easily by a positive bias. However, positive charges generated under high field positive bias (substrate injection case) are difficult to de-trap. Unique polarity dependence of HfO_2 appears to be due to two different defect mechanisms both generating positively charged states, but the physical origin of them are different.

Conclusion:

Stress polarity independent V_{th} shift of HfO_2 pMOSFET has been investigated. Positively charged defect states are generated during both gate injection and substrate injection stress. However, N_{it} generation and relaxation behaviors are quite different depending on a stress polarity and a magnitude of stress field. Silicon incorporation into HfO_2 effectively reduced electron related positive charge generation. Physical origins of these defect states need further investigation.

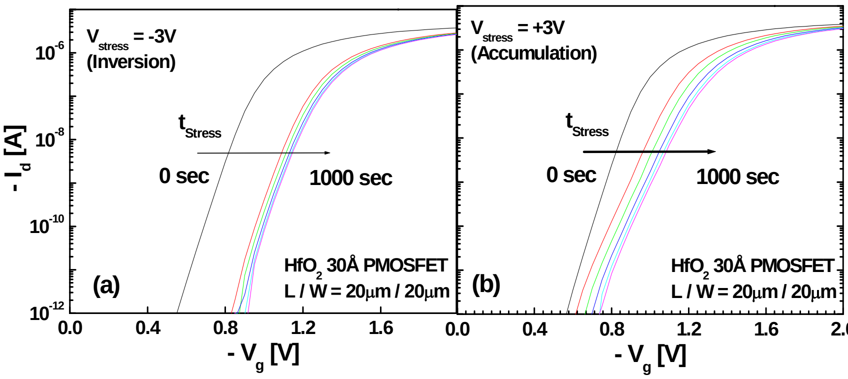

Fig. 1 Drain current versus gate voltage (I_d- V_g) characteristics of 30Å HfO_2 pMOSFET (a) During negative stress (-3V) and (b) positive stress (+3V)

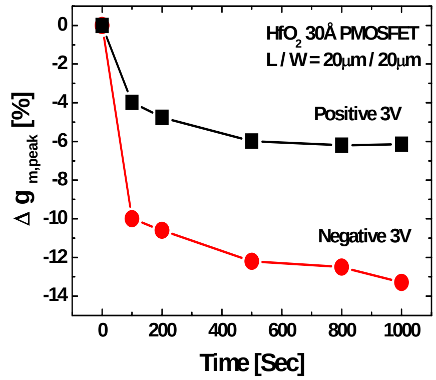

Fig. 2 Transconductance degradation rate for negative and positive stress

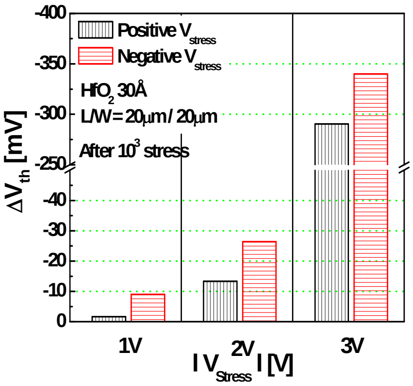

Fig. 3 Summarized threshold voltage shift of HfO_2 pMOSFET during positive and negative stress

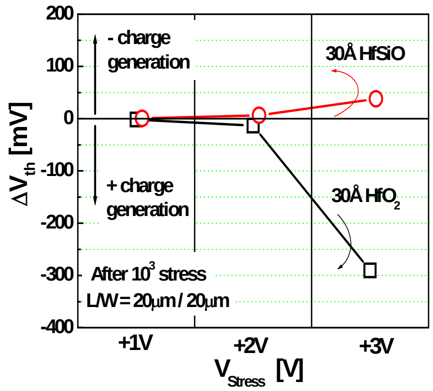

Fig. 4 Summarized threshold voltage shift of HfO_2 and HfSiO pMOSFET during +3V Stress

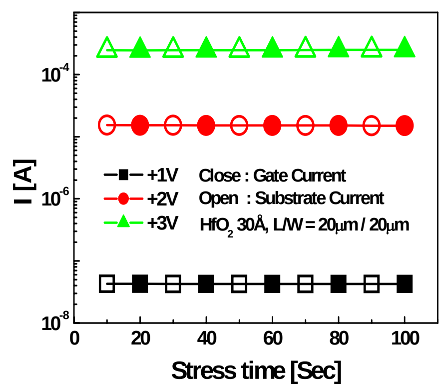

Fig. 5 Gate and substrate current during positive stress

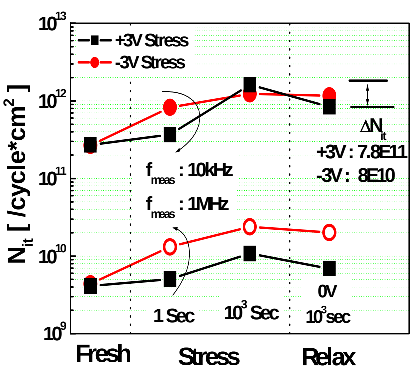

Fig. 6 Number of interface trap density during stress and relaxation

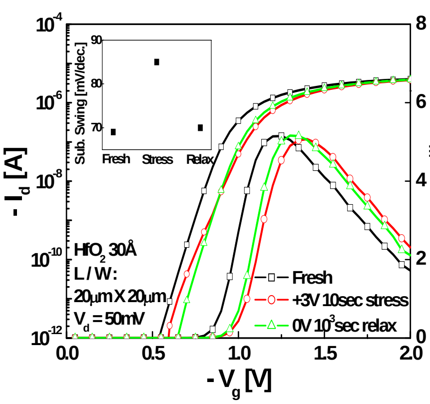

Fig.7 Id-Vg characteristics and subthreshold Swing degradation after stress and relaxation

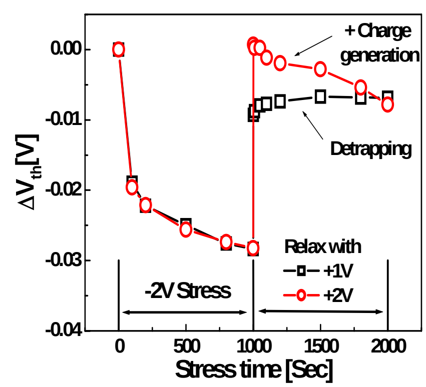

Fig. 8 Relaxation voltage dependent threshold voltage shift

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