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Highly Manufacturable Hf-silicate Technology with Optimized Composition for Gate-First Metal Gate CMOSFET

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Abstract

Effects of composition in Hf-silicate are evaluated for CMOSFET with TiN gate. Higher k value can be achieved by reducing Si content, effective to improve EOT-Jg performance. Lower Si content is also beneficial in terms of PMOS Vt variation caused by B diffusion. However, enhanced transient charge-trapping effect (TCE) is observed from Hf-silicate with low Si content, degrading electron mobility. Hf-silicate with low Si content also shows more TCE during positive bias stress at low stress bias, which is easily de-trapped. More permanent damage is observed in the Hf-silicate with high Si content due to relatively larger amount of SiO_2 portion in the film. TCE is reduced significantly when Hf-silicate scales aggressively ($T_{physical} \leq 3$nm), espcially for low Si content. For high performance application, scaled Hf-silicate with low Si content is desirable due to thinner EOT and less TCE.

Introduction

The Si and Hf concentrations in HfSiO have been studied extensively in terms of Fermi level pinning, crystallization and device performance/reliability for polysilicon gate CMOS devices [1,2]. However, there is no clear consensus on the optimal Si or Hf concentration in HfSiO for polysilicon gate CMOSFETs. Lower Si concentration is preferred in order to increase dielectric constant (k) [3]. But, more recent literature evinces a preference for higher Si concentration to reduce the Fermi level pinning effect [4] and to improve the performance and reliability of polysilicon gate CMOSFETs [5]. On the other hand, metal gate MOSFETs are different from poly silicon gate MOSFETs in terms of mobility, Fermi level pinning and process integration. The effects of Si or Hf concentration in HfSiO are not well understood for metal gate CMOSFETS, yet. This paper explores the effects of Si concentration in HfSiO on performance and reliability of CMOSFETs with TiN gate.

Experiment

Fig.1 describes the CMOS process flow used in this experiment. 3~4.5nm HfSiO was deposited on a Si (100) surface cleaned by ozonated DI water. Atomic layer deposition (ALD) was used for HfSiO deposition using precursors $Hf[N(CH_3)C_2H_5]_4$ and $Si[N(CH_3)C_2H_5]_4$ with O_3 as the oxygen source. HfSiO samples with 20%, 40% and 60% Si content were made, as confirmed by RBS analysis. 700ºC NH_3 post deposition anneal was performed to incorporate N into HfSiO (~7%). 10nm TiN was subsequently deposited using $TiCl_4$ and NH_3 in ALD chamber, followed by 150nm α-Si capping layer deposition. A conventional gate-first CMOS process flow was used with 1000ºC 5sec RTA after S/D implantation. After the whole process, forming gas anneal (FGA) was performed at 480°C for 30min.

Results and Discussions

It is well known that the k value increases as the Si content decreases in Hf-silicates, resulting in smaller EOT at a given physical thickness [1]. This is also observed in a TiN/HfSiO stack, as shown in Fig.2 (a). No significant difference in leakage current is observed (Fig.2 (b)), due to identical physical thickness. Fig.3 shows a monotonic EOT increase with Si % in HfSiO. Effective k value, calculated based on EOT and physical thickness, is over 11 for a Si 20% sample.

Fig.4 (a) and (b) show long channel Vt distribution of NMOS and PMOS respectively. A significantly wider PMOS Vt distribution is observed as the Si % increases, whereas NMOS shows tight Vt distribution regardless of the Si content. The intrinsic Vt values of N and PMOS are plotted against Si content in Fig.5. Both N and PMOS Vt increase linearly with increasing Si %, as expected because of the linear EOT variation. There is no indication of Fermi level pinning, because such pinning would presumably vary with the Si %, and the curves in Fig. 5 would then not be linear. Moreover, parallel Vt shift (absolute values) of N and PMOS with Si % also indicates Fermi level pinning is not occuring. The wide Vt distribution of PMOSFET is attributed to B diffusion from the α-Si capping layer through the TiN layer and into the HfSiO layer. The B in HfSiO may act as a positive charge, shifting the PMOS Vt in the negative direction [6]. The profile of B incorporated in HfSiO appears to be dependent on the amount of Si in HfSiO, as shown in the SIMS profile (Fig.6). It's clear that B tends to pile up at the interface of HfSiO/Si substrate when less Si is present in HfSiO films. The difference in B profiles with different Si content can be explained by N profile in HfSiO (Fig. 7). N is known to bond preferentially to Si in HfSiO film that is more available closer to Si substrate [7]. The N bond to Hf near the top surface could be easily decomposed and diffused out [7]. A relatively low and flat N profile in Si 60% results in higher [B] (with more gradual decline) in HfSiO. As more B exists in HfSiO bulk in Si 60% sample, more positive charges are generated, shifting Vt more negative. B diffusion through TiN could be due to its columnar grain structure as shown in cross section TEM (Fig.8).

Even though less Si % is preferred for its higher k value and smaller PMOS Vt variation, higher Si content in HfSiO improves the DC electron mobility significantly, especially the peak mobility values, as shown in Fig.9. Higher DC mobility with high Si content is attributed to less transient charge-trappping effect (TCE) during the Id-Vg measurement. The drain current drops during pulsed Id-Vg measurement, an indication of TCE [8], as shown in Fig.10. Higher Si content in HfSiO leads to a reduction in the TCE. Clearly, for HfSiO with low Si %, EOT reduction due to the higher k is offset by the mobility degradation due to higher charge trapping. TCE becomes much less as HfSiO thickness scales down to 3nm (Fig. 11), especially significant for HfSiO with low Si %. Scaled HfSiO with low Si % is, therefore, preferred to reduce EOT and TCE simultaneously for high performance application, once the gate leakage is tolerable.

Fig.12 shows positive bias instability (PBI) test on HfSiO with 20% and 60% Si. At low stress bias, higher Vt shift is observed for low Si% due to enhanced TCE through lager HfO2 portion in HfSiO. At high bias, however, high Si% sample shows gradual Vt rising with incomplete relaxtion as stress cycle increases. Fig.13 (a) and (b) show a top TEM view of Si 20% and 60% HfSiO. Due to phase separation, bright crystalline HfO_2 islands are observed within an amorphous SiO_2 matrix. The HfO_2 islands are smaller in the higher Si % samples. Incomplete Vt restoration during the relaxation step in PBI testing (high stress bias on high Si %) may be due to permanent damage to the SiO_2 portion of HfSiO as illustrated in Fig.12 (c). Less Si % is desirable to reduce permanent damage to the HfSiO.

Conclusion

Si content in Hf-silicates should be optimized depending on the requirement of the device for the specific application. Lower Si % in Hf-silicate results in a higher k value, but degraded mobility due to transient charge-trapping effect (TCE), whereas higher Si % shows less transient charging effect (thus higher DC mobility) despite its relatively low k value. Scaled HfSiO ($T_{physical} \leq 3$nm) with low Si % reduces TCE significantly, which is suitable for high performance application due to thinner EOT and less TCE. Less Si % is also desirable to reduce permanent damage during electrical stress.

References

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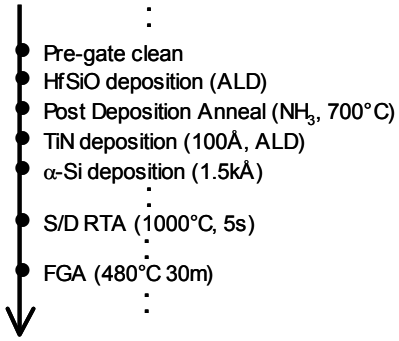

Fig.1 Brief Process flow. Conventional CMOS flow was used with High-K/Metal gate stack.

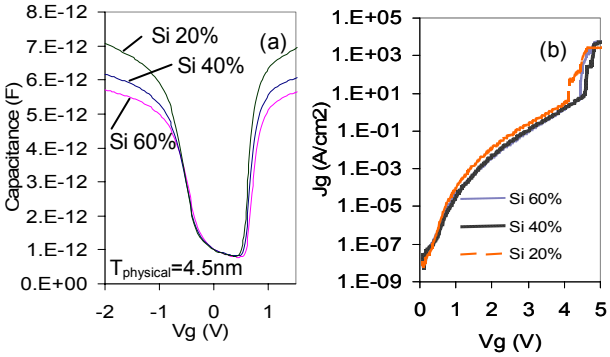

Fig.2 (a) C-V and (b) Jg-Vg curves of TiN/HfSiO stacks with different Si %. As Si % decreases, capacitance increases, without increasing leakage current

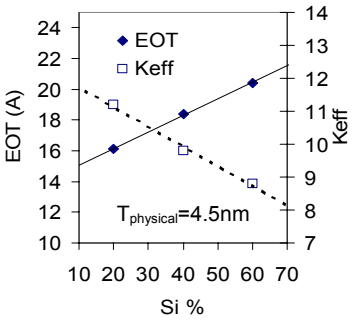

Fig.3 As Si % increases, EOT increases monotonically. Effective k values are calculated based on EOT and fixed physical thickness of 45Å

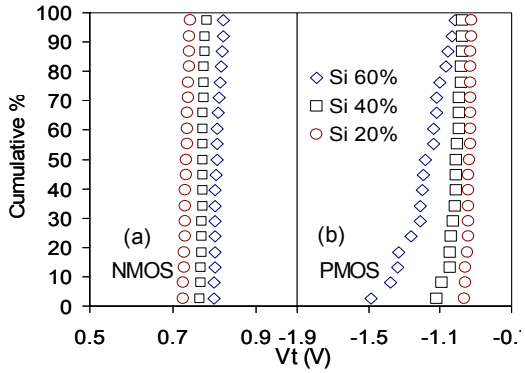

Fig.4 Vt distribution on the wafer from 10/1μm (W/L) device (a) NMOSFET, (b) PMOSFET. Significantly wider distribution is found as Si % increases, whereas NMOS shows tight distribution regardless of Si %

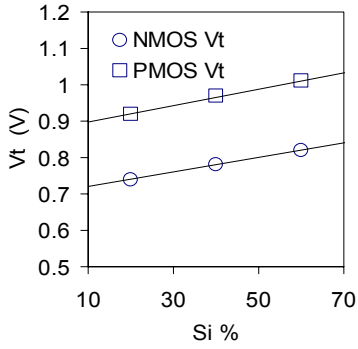

Fig.5 Intrinsic Vt dependency on Si % in HfSiO. Linear increasing of Vt with increasing Si % suggests no fermi level pinning. Increasing EOT is considered as a reason for increasing Vt

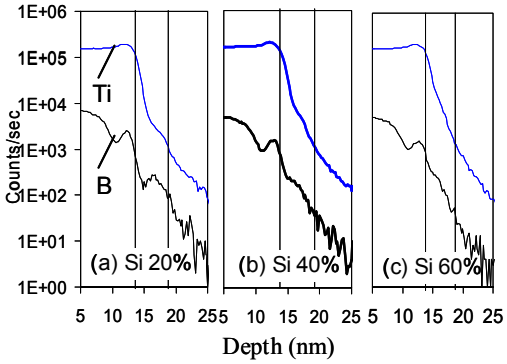

Fig.6 B and Ti profile with respect to Si % in HfSiO (a) SiO_2 20%, (b) SiO_2 40%, and (c) SiO_2 60%

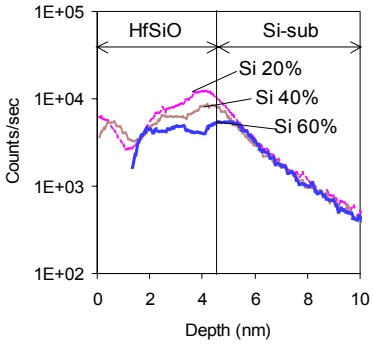

Fig.7 N profile in HfSiO with respect to Si %. As Si% decreases, N tends to move toward the HfSiO/Si interface and pile up.

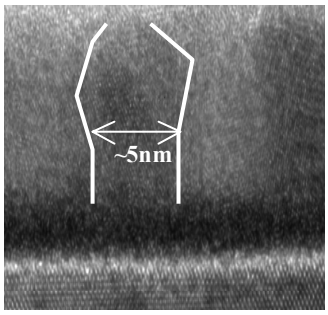

Fig.8 TEM cross section of TiN/HfSiO gate stack. Columnar grain structure of TiN is shown in the picture

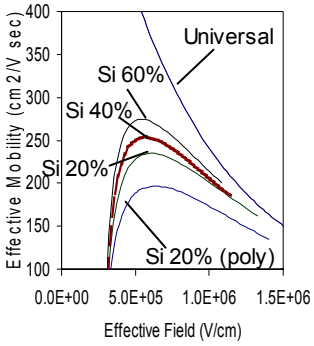

Fig.9 Electron mobility of TiN/HfSiO stack with different Si %. As Si % decreases, peak mobility increases.

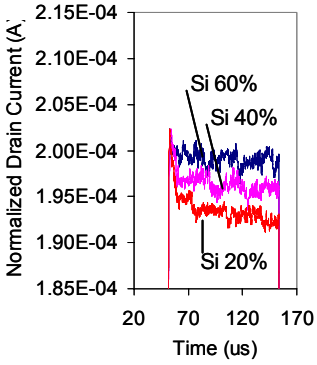

Fig.10 Normalized drain current drop during pulsed Id-Vg measurement results. High Si % in HfSiO improves mobility

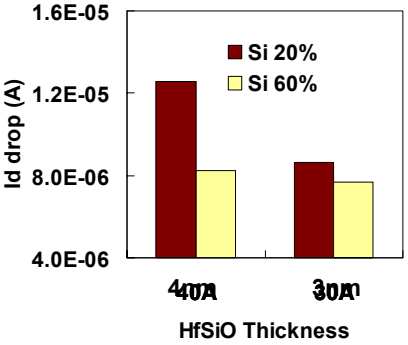

Fig.11 Drain current drop (during pulsed Id-Vg test) with respect to different HfSiO thickness with different Si %. Charge trapping becomes much less as thickness scales, especially significant for HfSiO with low Si %.

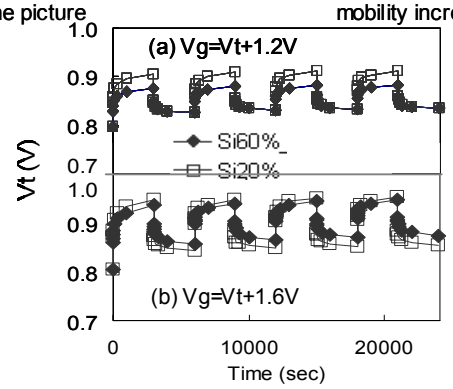

Fig.12 Positive Bias Instability (PBI) test on HfSiO with 20% and 60% Si. (a) as Si% increases, less Vt shift is observed at low stress bias. (b) at high bias, high Si% sample shows gradual Vt increase as stress cycle increases

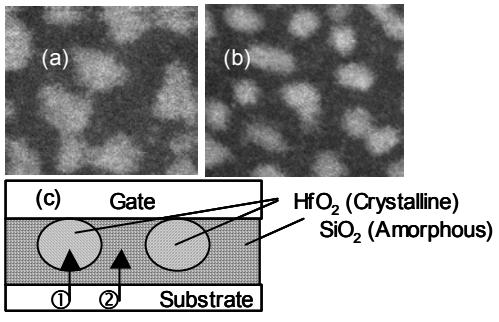

Fig.13 Top TEM view of (a) HfSiO (low Si%) and (b) HfSiO (high Si%). (c) illustrates cross section of the stack ① indicates Fast Transient Charging to HfO_2, and ② indicates injection to SiO_2, which possibly generate permanent damage