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Innovative Al Damascene Process for Nanoscale Interconnects

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1. Introduction

As the Silicon processing technology node goes to 60nm beyond, BEOL dimensions is required to aggressively scale down to meet performance target. But established Al RIE technology has been suffering from inherent issue such as photoresist pattern collapse, reliability deterioration of the metal wires by increase of lines stress and insufficient IMD gap-fill capability. One of the alternative candidate materials for metal line, W, could be problematic due to high line resistance and parasitic capacitance. It is expected that Cu metallization will have the scaling limits by electrical size effect[1]. For the reason, we have proposed that Al damascene process could replace the Al RIE that could result in better electrical and physical property. However, development of Al damascene process has difficulties in achieving stable and void free Al fill capability and obtaining scratch and corrosion free Al surface.

In this paper, we have made its appearance by bottom up growth of CVD-Al using Methylpyrrolidine Alane(MPA) precursor[2]. We observed that excellent Al filling capability in 40nm trench and confirmed robustness of Al damascene process using thermal cyclic test at 250 ℃ for 300hr. Furthermore, we compared electrical resistance of Al damascene with Cu damascene with various line dimensions.

2. Experimental

The single damascene pattern was fabricated with trench having 70nm to 40nm in width and ~ 7.5:1 aspect ratio. The process sequence of Al fill was (1) CVD-TiN deposition (2) PVD-TiN deposition as a stacked wetting layer (3) CVD-Al deposition by using Methylpyrrolidine Alane(MPA) precursor (4) PVD-Al deposition, and (5) Reflow. Lastly, the Al surface was polished by (6) 2-step CMP with colloidal silica based slurry. This procedure was as follows. The 1st step was for the bulk Al with highly selective slurry, and the 2nd step was for the cure of defects and topography with corrosion inhibitive and non-selective slurry, resulting in successful integration[3]. For comparison, Cu damascene process was carried out by deposition of RF 50Å/Ta 150Å/TaN 100Å, followed by seed and EP Cu deposition. W damascene process was achieved with CVD-TiN barrier metal of 70Å and CVD-W deposition.

SEM was used for Al fill characterization and Al surface characterization. The crystallography of Al structure in trench was analyzed by TEM. Electrical property was measured on the string pattern of a single damascene with 1600μm in length. The thermal stability was evaluated by annealing Al damascene pattern at 250℃ for 48hr in every cycles and measuring the line resistance.

3. Results and Discussion

Conventional CVD-Al process is not able to achieve a complete Al fill in sub-100nm trench pattern giving rise to a void making a pinch off at opening of damascene structure by overhang growth of CVD-Al as shown in Fig. 1. Accordingly, we have used a selective deposition technique of CVD-Al, in which the deposition rate of CVD-Al depends on the property of wetting layer. PVD-TiN/CVD-TiN stack structure was applied to induce selective growth at the trench bottom. Fig. 2 is a schematic sequence of bottom up growth of CVD-Al developed in this study. The control of thickness of PVD-TiN is highly important to provide a optimal surface condition for CVD-Al growth where Al can grow perpendicularly upward from the trench bottom and the growth on the sidewall become retarded, so called “bottom up growth”. Fig. 3 represents growth of CVD-Al in damascene pattern as the deposition time is elapsed. Fig. 4 is cross-sectional SEM micrographs of the Al and Cu fill features in damascene pattern showing excellent filling capability at 40nm. TEM pictures of Fig. 5 show polycrystalline structure of Al inside trenchs. Due to competing grain growth mechanism at the bottom of trench, cross section of trench may have grain boundaries which is parallel to the top surface. The perpendicular grain boundaries on trench surface between two trenchs also indicate that the grains grow in “bottom up growth” mode. Fig. 6(a) represent a dependence of the resistivity of Al and Cu damascene on line width. The resistance of Cu damascene structure significantly increase as the line width is scaled down to 50nm due to its sidewall scattering effect whereas Al damascene shows slow linear increase of line resistance. In addition, comparison result of electrical property clearly shows that Al damascene process has 1.5 times lower resistance than Al RIE as shown in Fig. 6(b). Based on the data obtained on the electrical resistivity of nano-scaled Cu and Al lines, we speculated that Al damascene structure using "BUG" could sustain good electrical property comparable to Cu damascene beyond 40nm interconnects. Further studies are presently underway to investigate on the evaluation of Al damascene process using various barrier metals such as CVD-W and Ru for improving the line resistance.

Finally, we proved that Al damascene process was reliable at repeated thermal cycle at 250℃ for 300hr without any degradation in the line resistance in Fig. 7.

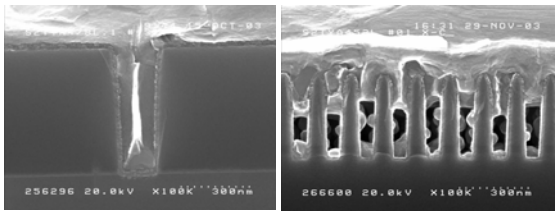
4. Conclusion

Al damascene process can extend Al metallization up to the sub-40nm interconnects for future devices. CVD-Al process using MPA precursor was developed to fill damascene interconnect by using a selective CVD-Al

deposition property on stacked films of PVD-TiN and CVD-TiN making bottom up growth of CVD-Al, and resulted in excellent electrical properties. We believe that Al damascene can replace Al RIE, and can be applied in future interconnect technologies.

5. References

[1] G. Steinlesberger et al., *IITC* P51, 2004.
[2] S. H. Han et al., *MRS 2005 Spring Meeting*, V863.
[3] J. H. Park et al., *AVS 6th ICMI* 2005.



(a) (b)

Fig. 1. Cross-sectional SEM micrographs of the Al fill features in damascene pattern by conventional CVD-Al process at (a) 120nm in width, 400nm in height, and (b) 70nm in width.

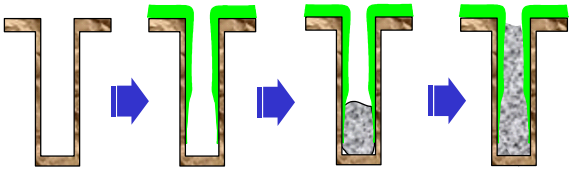


Fig. 2. Schematic sequence of trench fill process by bottom up growth of CVD-Al.

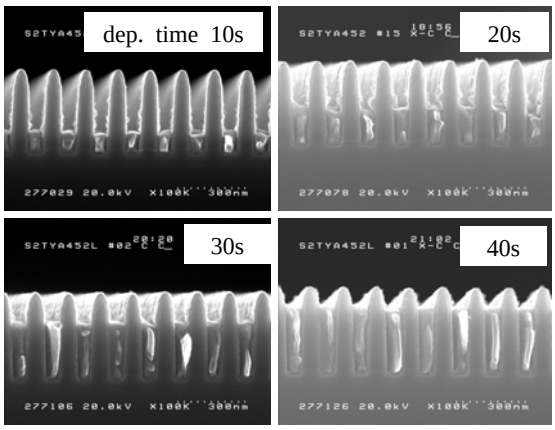
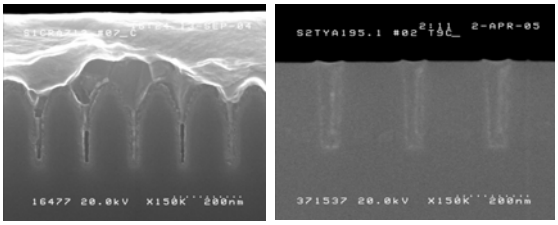
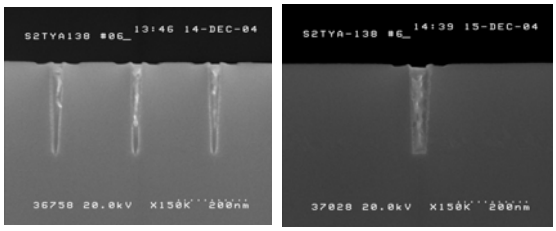


Fig. 3. Cross-sectional SEM images of bottom up growth of CVD-Al as the deposition time is elapsed.



(a)



(b)

Fig. 4. Cross-sectional SEM micrographs of the (a) Al and (b) Cu fill features in damascene pattern at 30nm and 50nm line width, respectively.

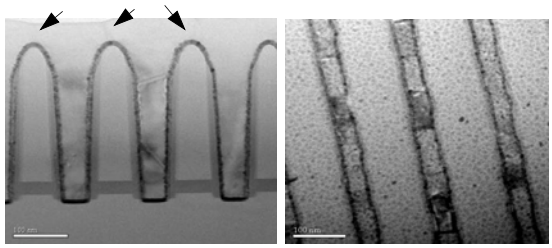
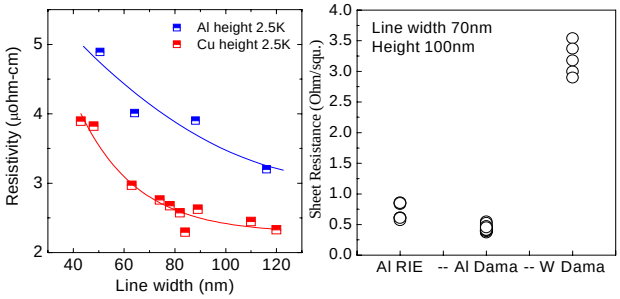


Fig. 5. TEM micrographs of CVD-Al microstructure of "BUG" in damascene.



(a) (b)

Fig. 6. Dependence of (a) the resistivity on line width from Al and Cu damascene, (b) line resistance of Al schemes and W damascene.

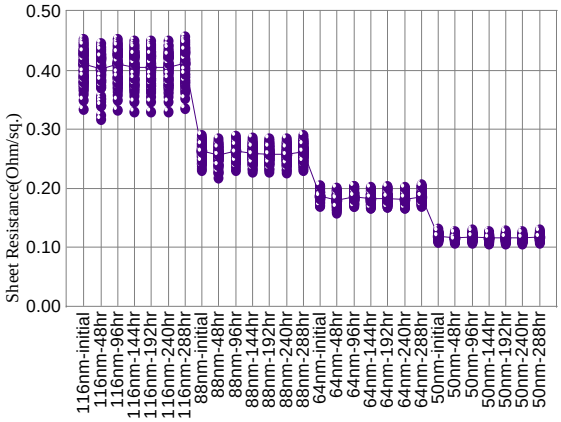


Fig. 7. Line resistance of Al damascene in repeated thermal cycle at 250℃ for 300hr on line widths.