Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.64-65

C-2-3

New Three-Dimensional Integration Technology Using Chip-to-Wafer Bonding to Achieve Ultimate Super Chip Integration

Takafumi Fukushima, Yusuke Yamada, Hirokazu Kikuchi, and Mitsumasa Koyanagi

Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University
6-6-01 Aza Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, 980-8579, Japan.
Phone: +81-22-795-6906; Fax: +81-22-795-6907; E-mail: sdlab@sd.mech.tohoku.ac.jp

1. Introduction

Three-dimensional (3D) integration is the most promising technology to improve LSI performance by reducing wiring delay and increasing interconnection density. We have previously reported and fabricated 3D LSIs based on wafer-to-wafer bonding [1], [2]. However, the wafer-level 3D integration has serious disadvantages such that chip yield is exponentially decreased with the number of stacking layers. In this study, we newly proposed 3D integration technology based on chip-to-wafer bonding, called ultimate super chip integration, which has a possibility to realize 3D LSIs with high yield and low cost.

2. Concept of ultimate super chip integration

Figure 1 shows the conceptual viewgraph of ultimate super chip integration. After wafer probing and dicing, good dies for the first layer such as processors are arrayed and bonded on a support wafer. Good dies for the second layer such as memories are then stacked on the first dies. We can obtain multiple stacked 3D LSIs based on chip-to-wafer bonding by repeating this sequence. The most striking characteristic of ultimate super chip integration is that dies with various sizes and several kinds of devices such as sensors can be stacked, and they are electrically and vertically connected with buried interconnections.

3. Fabrication processes of multiple stacked 3D LSIs

Processes to fabricate multiple stacked 3D LSIs based on ultimate super chip integration are schematically shown in Fig.2. First, CMOS chips for the first layer are arrayed and bonded on a Si wafer, followed by injection of low-viscosity adhesion into the resulting extremely narrow gap between the chips and the wafer. A high-viscosity resin with low coefficient of thermal expansion (CTE) is then coated on the arrayed chips so as not to generate their edge-chipping in the following process, where the chips are thinned until buried interconnections appeared. After that, Au/In bumps are formed on the buried interconnections by a lift-off technique. Then, CMOS chips for the second layer are precisely aligned and bonded in the similar manner. Repetition of this process sequence affords multiple stacked 3D LSIs with a variety of chip sizes and functions.

4. Results and discussion

24 pieces of dies (7 × 7mm) with vertical interconnections filled with n^+ poly-Si (0.4 mΩ cm) were arrayed on a Si wafer at 200-μm intervals by flip-chip bonding as shown in Fig.3(a). Figure 3(b) shows a cross-sectional view of a bonded die and the neighboring die, where vertical interconnections in depth of 60 μm and the width of 2-3 μm can be observed. A low-viscosity adhesion was then readily injected into the resulting gap about 4 μm in thickness by capillary force and differential pressure. As shown in Fig.4, it takes approximately two minutes to fill a few microns of a gap between an upper dummy glass chip (5 × 5mm) and a lower Si wafer with an appropriate droplet of the adhesion at atmospheric pressure by capillary force alone. This adhesion injection is an effective method for a considerable reduction in time required to assemble 3D LSIs. Low-CTE resins are indispensable materials for the following grinding processes to give uniformly thinned chips without edge-chipping. Figure 5 shows the warpage-related characteristics of a heat-curable resin with fillers used in this study. Compared with an UV-curable resin without fillers, warpage was little caused by the coating of the heat-curable resin. Comparison of tightly bonded dies before and after thinning is shown in Fig.6. The dies with their initial own thickness of ~280 μm were thinned to around 40 μm by grinding and chemical mechanical polishing (CMP). As shown in this figure, the buried interconnections, 2 μm width and 12 μm length, clearly appeared. After the formation of evaporated Au/In bumps on the buried interconnections by a lift-off technique, the second layer of dies with different sizes were precisely mounted by mechanical alignment. By repeating this sequence, three-layer dies with various sizes were successfully stacked in an alignment error of within several microns as shown in Fig. 7.

5. Conclusion

A novel chip-to-wafer 3D integration technology of ultimate super chip integration was introduced. The process sequence of ultimate super chip integration for realization of multiple stacked 3D LSIs was demonstrated. This integration technology would be applied to fabrication of an advanced high performance LSIs.

Acknowledgements

We would like to thank the staffs of the Venture Business Laboratory, Tohoku University, Japan.

References
[1] T. Matsumoto, M. Sato, K. Sakuma, H. Kurino, N. Miyakawa, H. Itani, and M. Koyanagi, *Jpn. J. Appl. Phys.,* **37**, 1217 (1998).
[2] K.W. Lee, T. Nakamura, K. Sakuma, K.T. Park, H. Shimazutsu, M. Miyakawa, K.Y. Kim, H. Kurino, and M. Koyanagi, *Jpn. J. Appl. Phys*., **39**, 2473 (2000).

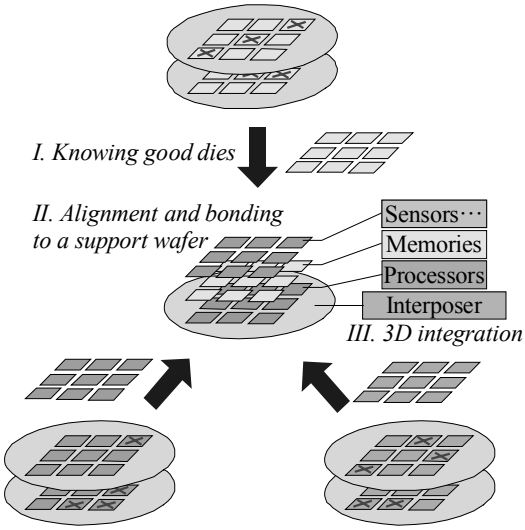


Fig. 1 Conceptual viewgraph of ultimate super chip integration.

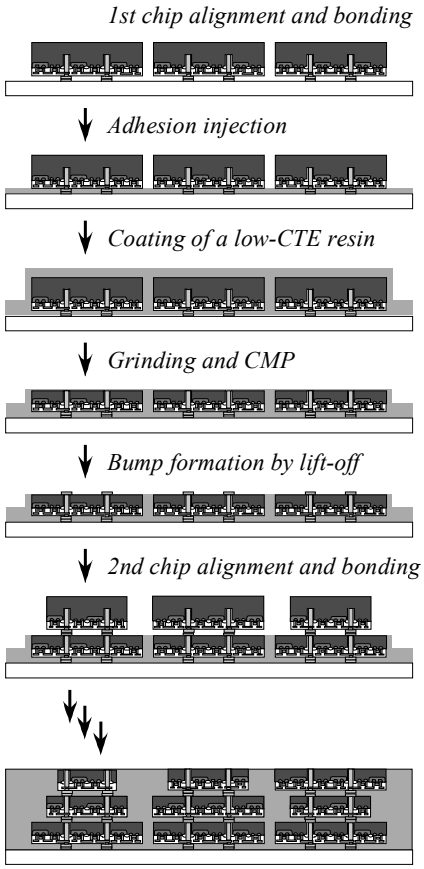


Fig. 2 A fabrication process of three-dimensionally stacked LSIs based on ultimate super chip integration.

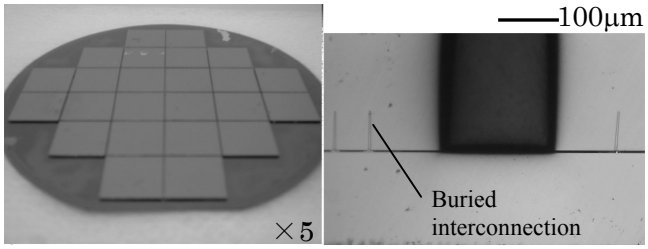
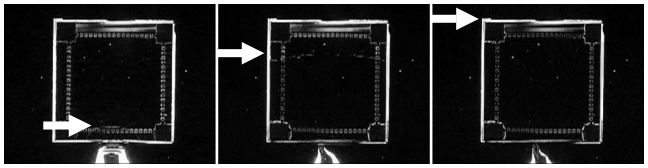


Fig. 3 Photomicrographs of the top (left) and cross-sectional (right) view of the first layer of stacked dies on a support wafer.



(a) 0:00 min (b) 1:02 min (c) 1:55 min

Fig. 4 Frames of an adhesion injection event from a video taken at a microscope at atmospheric pressure: glass-chip dimensions are 5 × 5mm.

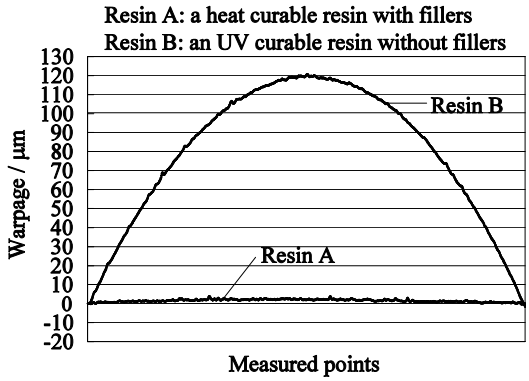


Fig. 5 The warpage generated by curing of resins with a thickness of ~70μm on Si wafer.

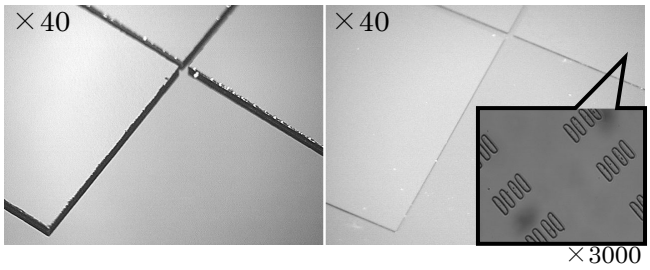


Fig. 6 Comparison of dies before and after thinning by grinding and CMP, and a photograph of appeared buried interconnections (upper right corner).

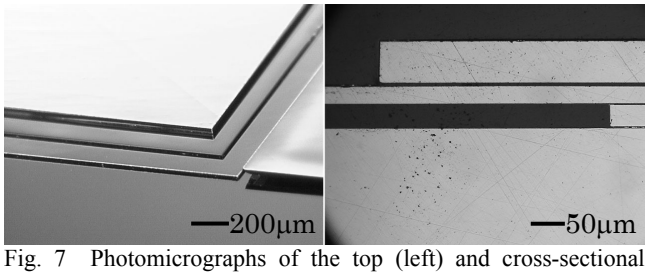


Fig. 7 Photomicrographs of the top (left) and cross-sectional (right) view of three-layer stacked dies based on ultimate super chip integration.