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Characteristics of Silicon-on-Low-K Insulator (SOLK) MOSFET with Metal Back-Gate

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1. Introduction

Higher performance and lower power consumption have been required for small size devices used in advanced LSI's. One of the most effective ways to achieve higher performance and lower power consumption in MOSFETs with small dimension is to vary the threshold voltage (V_{th}). Both high performance and low power can be achieved by decreasing the threshold voltage in on-state and increasing it in off-state. The back-gate is very effective for controlling the threshold voltage. Another way to achieve high performance and low power consumption is to employ the fully depleted (FD) SOI MOSFET with superior subthreshold characteristics and smaller parasitic capacitance. Then, we have announced a new FD-SOI MOSFET with buried back-gate which is formed by ion implantation through the SOI layer and the buried oxide into the Si substrate surface region underneath the buried oxide [1]. However, the controllability of threshold voltage was not sufficient due to the surface depletion of back-gate region with relatively low impurity concentration. Therefore, the metal gate is necessary even for the back-gate. In addition, the signal propagation loss related to the Si substrate is a big concern in a high frequency operation although the parasitic capacitances are reduced by SOI structure. Therefore, we have proposed a new technology to employ a low-k material as a substrate which is called SOLK (Silicon-On-Low-K substrate) to eliminate the signal propagation loss related to the Si substrate and more dramatically reduce the parasitic capacitances [2]. In this work, we propose a new SOLK MOSFET with metal back-gate to achieve higher performance and lower power consumption by employing both the SOLK structure and the metal back-gate.

2. Experimental

Figure 1 shows the cross-sectional structure of the SOLK MOSFET with metal back-gate. As is clear in the figure, the SOLK MOSFET has the structure in which FD-SOI MOSFET wafer is face-down bonded onto a handle wafer and the Si substrate of SOI wafer is completely removed. The metal back-gate is formed on the buried oxide (BOX) above the front gate. The fabrication process sequence of SOLK MOSFET with metal back-gate is shown in Fig.2. First of all, we fabricated FD-SOI MOSFETs. The SOI wafer with the SOI film thickness of 50nm and the buried oxide thickness of 100nm was used as the starting wafer (Fig.2(1)). After the device fabrication, the adhesive layer was formed onto the SOI device wafer. A low-k material of Benzocyclobutene (BCB) was used as an adhesive material which can be used in the CMOS process. It is stable at the processing temperature up to 350℃ and gives rise to excellent planarization characteristics and good bondability to various kinds of materials. BCB was spin-coated onto the SOI device wafer and pre-cured in the nitrogen atmosphere (Fig.2(2)). Next, the device wafer and the handling wafer coated with the adhesive layer were installed in a high vacuum chamber of bonding machine to accelerate outgassing, face-to-face bonded and cured in the same chamber (Fig.2(3)). Then, the silicon substrate of SOI wafer was completely removed so as to expose the buried oxide (BOX) after wafer bonding. Tetramethyl ammonium hydroxide (TMAH) was used to remove the Si substrate. TMAH has the high etching selectivity of Si to SiO_2. Then, the buried oxide was used as the silicon etch stop (Fig.2(4)). Finally, after the formation of contact via through the buried oxide, the metal back-gate and the metal wirings were formed to complete the SOLK MOSFET with metal back-gate (Fig.2(5)).

3. Results and Discussions

Figure 3 shows the SEM micrograph of the fabricated SOLK MOSFET with metal back-gate. Al was used as a back-gate material. As is clear in the figure, the silicon substrate of the SOI wafer is completely removed and the metal back-gate is formed on the buried oxide above the front gate. Figures 4 and 5 show the drain current-voltage characteristics and the subthreshold characteristics of SOLK-NMOSFET and SOLK-PMOSFET with the gate length of 0.25μm varying the back-gate bias as a parameter. The back-gate voltage was swept from –3V to 3V. The threshold voltages are shifted to the positive voltage direction by applying the negative back-gate bias voltage whereas the on-currents are increased by applying the positive back-gate bias voltage in NMOSFET and the negative back-gate bias voltage in PMOSFET. Figure 6 shows the threshold voltages of SOLK-NMOSFET and SOLK-PMOSFET as a function of back-gate bias voltage. In the figure, the threshold voltages of SOI-MOSFETs with buried back gate are also plotted for the comparison. The modulation rate of threshold voltage to back-gate bias voltage was increased from 25mV/V to 55mV/V in NMOSFET and from 30mV/V to 35mV/V in PMOSFET by employing the SOLK-MOSFETs with metal back-gate in place of SOI-MOSFETs with buried back-gate. Thus, the metal back-gate is more effective for controlling the threshold voltage than the buried back-gate giving rise to larger immunity to the short channel effect (SCE).

Figure 7 shows the on-currents and off-currents of SOLK-NMOSFET and SOLK-PMOSFET as a function of

back-gate bias voltage. It is clearly seen in the figure that the on-current is significantly increased by applying the positive back-gate bias voltage in NMOSFET and the negative back-gate bias voltage in PMOSFET whereas the off-current is decreased by applying the negative back-gate bias voltage in NMOSFET and the positive back-gate bias voltage in PMOSFET.

4. Conclusion

A new SOLK MOSFET with metal back-gate has been proposed and successfully fabricated using wafer bonding method with low-k material as an adhesive. The SOLK MOSFET with metal back-gate has the possibility to achieve higher performance and lower power consumption. It was shown that the threshold voltage, the on-current and the off-current are more effectively controlled by the back-gate bias voltage in SOLK-MOSFETs with metal back-gate than in SOI-MOSFETs with buried back-gate.

References

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[2] Y. Yamada, Y. Igarashi, T. Morooka, T. Nakamura, J. C. Shim, H. Kurino and M. Koyanagi, *Ext. Abstr. 2002 Int. Conf. Solid State Devices & Materials p.316*

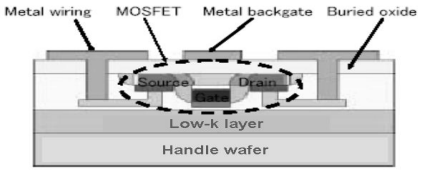


Fig. 1 Cross-sectional structure of SOLK-MOSFET with metal back-gate.

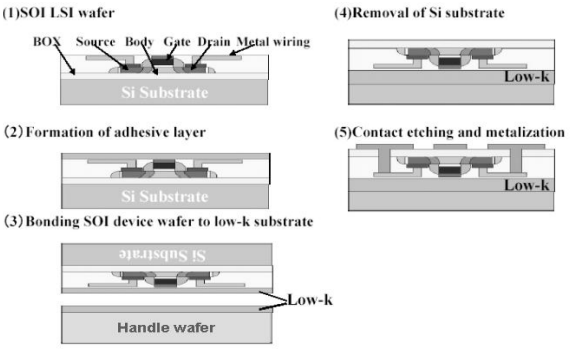


Fig. 2 Fabrication process flow.

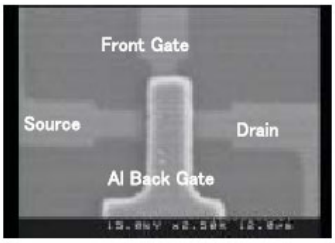
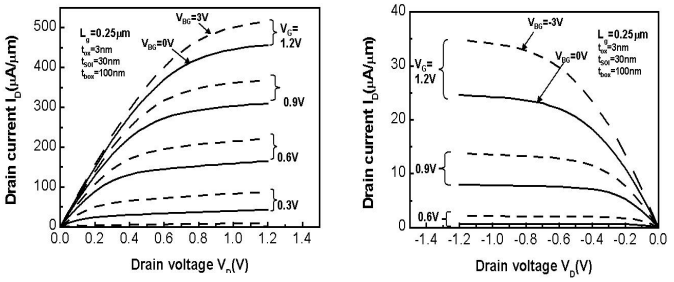
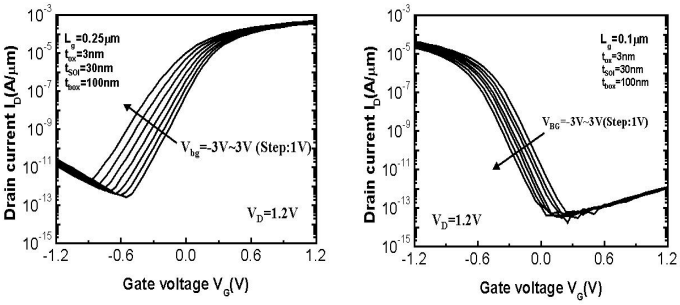


Fig. 3 SEM micrograph of SOLK-MOSFET with metal back-gate.



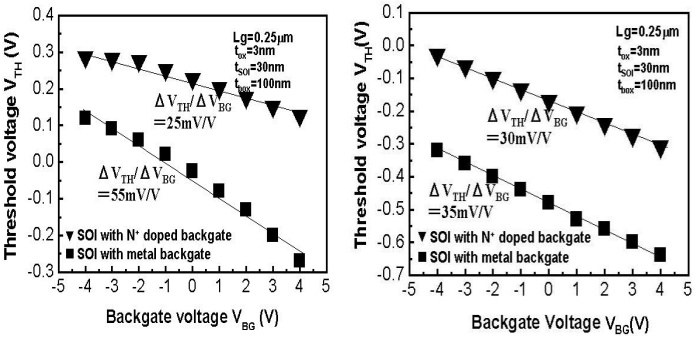
(a)NMOSFET (b)PMOSFET

Fig. 4 Drain current-voltage characteristics of SOLK-MOSFETs with metal back-gate.



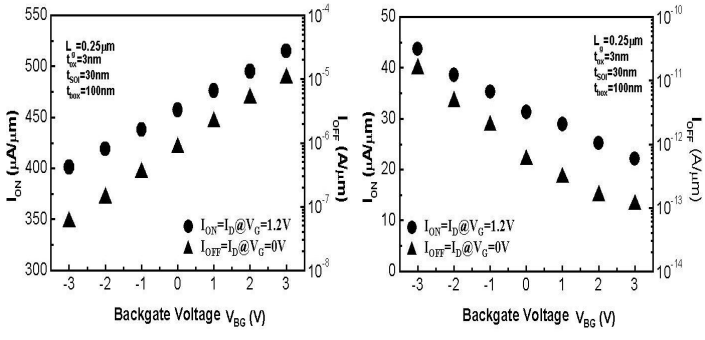
(a)NMOSFET (b)PMOSFET

Fig. 5 Subthreshould characteristics of SOLK-MOSFETs with metal back-gate.



(a)NMOSFET (b)PMOSFET

Fig. 6 Threshold voltages of SOLK-MOSFETs with metal back-gate and SOI-MOSFETs with buried back-gate as a function of back-gate bias voltage.



(a)NMOSFET (b)PMOSFET

Fig. 7 On-currents and off-currents of SOLK-MOSFETs with metal back-gate as a function of back-gate bias voltage.