Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.296-297

C-5-4

Width Scaling and Layout Variation Effects on Dual Damascene Copper Interconnects Electromigration

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1. Introduction

The reliability of Cu/low-k interconnects has become an important concern for the 0.13μm technology node and beyond. Cu electromigration(EM) is the key issue that limits the lifetime of advanced interconnect systems. However, few studies have reported on the effect from narrow to large lines on median time to failure (MTF). Therefore, the present study focuses on the wide range width effect. The especially suitable EM test structures to evaluate the properties of Cu were well designed. More real structures than pure metal line are designed using sufficient via to eliminate the via-limited fails. A possible theory was proposed to explain the result.

2. Experiment

The EM tests were carried out at the package level. Samples were fabricated using 90nm 300mm Cu dual damascene process. The TaN/Ta liner and Cu seed layers were deposited sequentially by using PVD method. In addition, re-sputtering leads to the excellent side wall coverage and void free in vias. Testing was conducted typically at 300 ^{o}C with a current density of 1.2~2.0 MA/cm^2. The EM failure criterion was defined as 10% of resistance increase or when extrusion monitor current exceeds 1μA. Figs. 1(a)-(c) are schematic diagrams of three-level interconnect structures discussed in this paper. Down-stream case defined for the electron flowing from upper wide metal line over via into the under narrow metal line was stressed.

3. Results and Discussion

Various widths of EM test structures were designed to evaluate the EM performance. The cumulative lifetime data for the 0.14μm to 0.42μm wide lines fitted by a log-normal distribution are shown in Fig.2 and the values of σ in the log-normal distributions, even in a wider line, are all quite similar. The median time to failure (MTF) was measured at different line widths, and the results are plotted in Fig.3(a). MTF decreases sharply as the linewidth increases in the range below 0.42μm. Voids, which grow at the bottom of via, cause the line to fail [1]. Due to large current crowding, and the lack of liner redundancy [2], design rule allowed maximum width with single via show worst case in MTF. To prevent the via-related process issue, dual vias are designed to relief the via-depletion mode. For 0.42μm wide line, three different via arrangements were designed i.e. rectangular via, dual via-row, dual via-column. More than three times MTF increase was compared with single via structure. The variation of MTF for different dual via designs is shown in Fig.3(b). It is obvious that wide line with dual via-row, which along the line length, the MTF is the longest due to requirement for large volume of Cu depletion. The MTF of rectangular via decreases around 20% than that of dual via-row. However, the underneath line width can be narrowed down for rectangular via. It is trade off between reliability and line routing area design. For 0.14μm narrow line, the MTF of dual via-row is around 1.6 times than that of single via. In comparison with 0.42μm wide line, the MTF of dual via-row increases 4.6 times than that of 0.42μm wide line with single via. It is interesting that the structure with dual via design the MTF of 0.42μm is very close to that of 0.14μm. The cases for 0.42μm wide line that single via limits the EM performance are eliminated. Fig. 4(a)-(b) are top view FIB images of 0.14 and 0.42μm wide Cu lines. A bamboo-like microstructure was found in 0.14μm Cu line, while a mixture of bamboo-like and polycrystalline was found in 0.42μm wide Cu line. The result further confirms that microstructure does not play a dominant role in the copper electromigration if the via-limited issue was eliminated. The cumulative lifetime data for the 1μm to 3.5μm wide lines are shown in Fig.5 and the values of σ, even in a wider line, are all about 0.3. The failure mode remains unchanged. SEM image for 1.68μm failure sample is shown in Fig.6. The void shape seems to indicate that the void probably started at the first via, and then void grew up to reach the second via. No void form directly under via bottom, like a very thin slit void, was found. It seems reasonable to assume that no via-limited issue degrades EM lifetime. The temperature coefficient of resistance (TCR) values have been investigated with regard to median grain size and the defectiveness of the crystal lattice, respectively. High TCR values indicate large median grain sizes, whereas smaller TCR correspond to a fine-grained microstructure [3]. The TCR value was found to increase monotonically with linewidth but to go through a maximum at w ~ 1μm and then slightly decreased to a constant value in Fig.7. Since thickness of the electroplated Cu file before CMP process is 1μm, the grain size is limited by deposition Cu thickness rather than by metal width. The MTF as a function of linewidth is plotted in Fig.8. MTF slightly increases with linewidth w but goes through a maximum at w ~ 1μm and then sharply decreases to a minimum at w =3.5μm. As w > 3.5μm, the MTF slightly increases to a constant value. The observed behavior of width dependency can be explained below. For polycrystalline line structure, the drift velocity can be written as [4]:

$$V_d=[\underbrace{(\delta_{GB}/d)(1-d/w)D^0_{GB}e^{(-Q_{GB}/kT)}Z_{GB}^*}_{(1)}+\underbrace{\delta_S(2/w+1/h)D^0_Se^{(-Q_S/kT)}Z_S^*}_{(2)}]e\rho j/kT$$

Where the subscript GB refers to the grain boundary; δ_{GB} denotes the width of grain boundary; d is the grain size; h is the thickness. For (2) part large w range, (2/w+1/h)~1/h, surface diffusion velocity are almost the same for large w region. However, for (1) part

w=1μm, the grain size d ~ 1μm, grain boundary diffusion term is neglected. So MTF reaches a maximum at w ~ 1μm. Since d is almost the same for w>1μm range, as the w increase, the grain boundary diffusion impact will increase. MTF sharply decreases to a minimum at w =3.5μm. When w > 5μm, dielectric slots are auto generated to prevent CMP dish effect; EM induced atom diffusion will be scattered by dielectric slot. MTF will slightly increase for w=6μm. EM behavior is absolutely different from w < 5μm.

4. Conclusions

Electromigration in dual damascene Cu line width effect has been investigated. The structures having sufficient via to eliminate the via-limited fails were designed. More reliable width scaling effect was demonstrated. There are two scenarios for width scaling effect. One is w<1μm region. MTF show weak width dependence except the via-limited condition. The other is w>1μm region. MTF show strong width dependence. Possible theory was proposed to explain the observed behavior. The study will provide some contribution to the development of line routing layout for robust EM design consideration.

References

[1] M. H. Lin et al., in *proc., IRPS.*, pp.229-233, 2004.
[2] B.-Z. Li et al., et al., in *proc.,IRPS.*, pp.140-145, 2003.
[3] A.von Glasow et al., in *proc., IRPS.*, pp.126-131, 2003.
[4] C.-K. Hu, et al., in *proc..AMC.*, 1999.

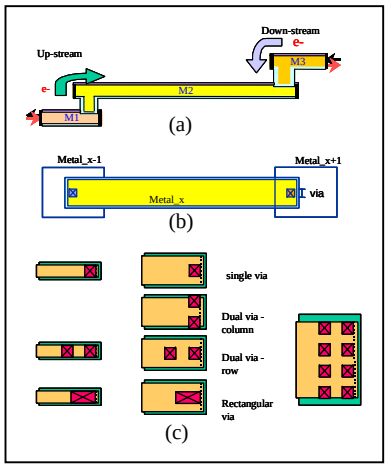

FIG 1. (a) Via terminated line structure. Downstream is evaluated. (b) Top view of wide line with single via. (c) Various EM structures for width dependence, left:w=0.14, middle w=0.42, right w>0.42μm

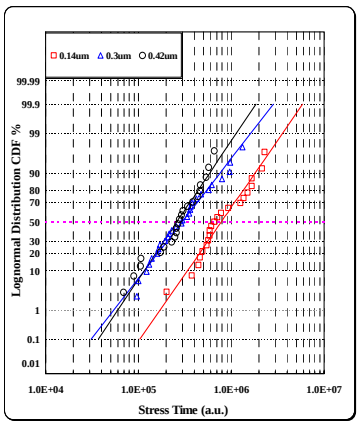

FIG 2. Lognormal Time-To-Failure distribution plots for w=0.14, 0.3, 0.42μm for down-stream case. Similar distributions are shown.

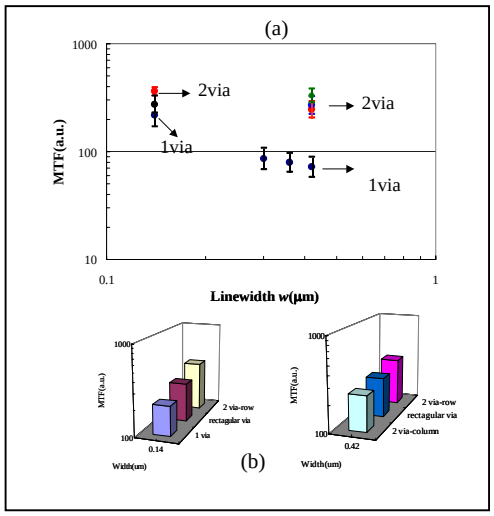

FIG.3 (a): Plot of MTF as a function of linewidth. 90% confidence levels are lower and upper bound. (b):2 via cases for 0.14 and 0.42μm, stress condition is the same for various structure.

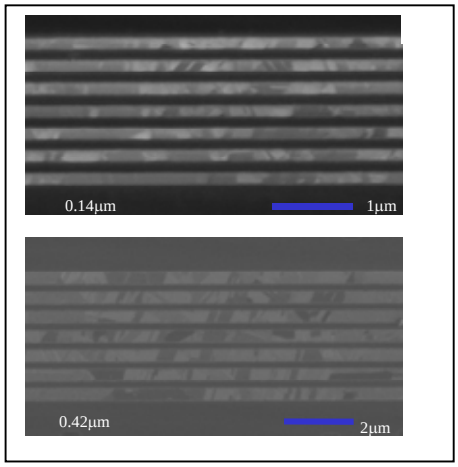

FIG 4. FIB images of 0.14μm(top) and 0.42μm(bottom) EM structures, bamboo like and mixture microstructure are shown.

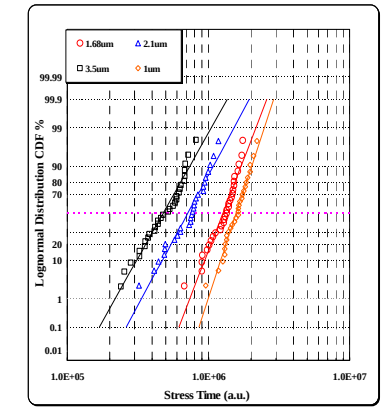

FIG 5. Lognormal Time-To-Failure distribution plots for w=1, 1.68, 2.1 and 0.42μm for down-stream case. Similar distributions are shown. Stress condition is the same.

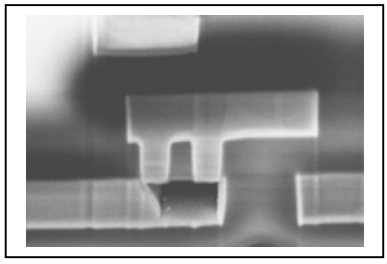

FIG 6. SEM image for w=1.68μm wide line structure, void was found in via bottom. Large trench void cross other via is depleted.

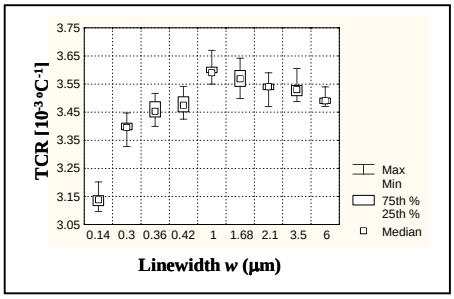

FIG 7. Plot of TCR value as a function of linewidth. It goes through a maximum at w ~ 1μm and then slightly decrease to a constant value.

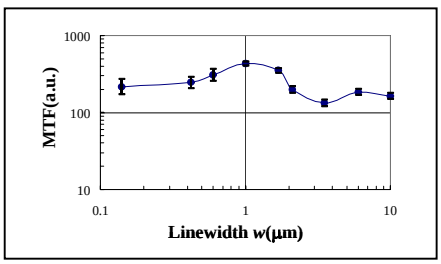

FIG 8. Plot of MTF as a function of linewidth. 90% confidence levels are lower and upper bound. For w>0.42μm, sufficient via are designed to relief the via-limited issue. Stress condition is the same.