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Via-Profile Controlled, Porous Low-k/ Cu DDIs with High Thermal Stability

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1. Introduction

To reduce cross-talk among the fine-pitched interconnects for the 65nm-node ULSI and beyond, the parasitic capacitance has to be decreased Dual damascene (DD) interconnects with low-k film are desirable for reducing the effective (k_{eff}), but it is difficult to control the complex structure of vias and line-trenches. By a conventional resist-mask process as shown in Fig. 1(a), fence is made around the top-opening of vias at the line-trench bottom because of ion-trajectory distortion by the negative charges on photo-resist followed by redeposit of by-products [1].

In this work, we investigate the effect of via profile on the thermal reliability, comparing between the via profiles of the tapered-vias and the fenced-ones in 65nm-node ULSIs (Fig. 1(b)). It is found that the controlled tapered-vias improve the thermal stability of Low-k/Cu DDIs.

2. Experimental

Double-layered, Cu-DDIs with a porous SiOCH film (k=2.6) were fabricated by two different fabrication processes [2, 3]. The tapered-vias were fabricated by Via-first Multi-hard-mask (VF-MHM) process, while the fenced-vias were obtained by Via-first Multi-resist (VF-MR) process as shown in Figs. 2(a) and (b), respectively. The via-bottom-diameter was fixed as $0.11\mu m^{\phi}$. Here, the lower line, the vias, and the upper line are notated as M1, V1 and M2, respectively. After fabrications of the Al pads and the cover film, the via resistances were measured in the 10k-chain with various widths of M1 and M2. High temperature thermal- cycle (T/C) tests were conducted between RT and 350 ^{o}C, at which the wafers were held for 30 minutes in one cycle. To understand the thermal stability depending on the via profile, the thermal stresses were simulated by 3D finite element analysis.

3. Results

Fig. 3 shows distributions of the via resistances fabricated by VF-MHM and VF-MR processes. The FIB-SEM images of vias are also shown. No difference in the via resistance was observed for both of the vias irrespective of their via profiles. Fig. 4 shows distributions of the change in the via resistance after 20 cycles of T/C test. The average resistance of the fenced-vias increased 8%, while the tapered-vias suppressed the resistance increment within 4%. By FIB/SEM observation, the voids in Cu were observed at the top-corner of fenced-vias (indicating “circle”), thus increasing the via resistance by the T/C test.

Fig. 5 shows the failure rates of 10k via-chain as a function of the line widths of M1 and M2 lines after the 20 cycle of T/C test. Here, 5% increment of the via resistance to the initial was defined as the via failure. In case of the 3μm-wide M2 lines (Fig. 5(a)), 100% of the fenced-vias were failed with the M1 lines wider than 0.8μm, while the failure of tapered-vias was suppressed within 10% to the 3μm-wide. In case of the 3μm-wide M1 lines (Fig. 5(b)), the via failure of the fenced-vias on the 0.14μm-wide, M1 lines was suppressed, but the failure rate was increased abruptly with widening the M2 line. In case of the tapered-vias, on contrast, the failure was kept within 15%.

It is found that the reliability of the tapered-via is superior to that of the fenced-via under the T/C test irrespective of the line widths.

4. Discussion

Fig. 6 shows the Mises-stress distribution simulated in the Cu DDIs at RT by assuming stress-free at a high temperature. It is found that high compressive stress is applied to the corner of the fenced-vias (indicating “arrow”). The position was well coincident with the voiding position at Cu DDI as shown in Fig. 4. No stress concentration, on contrast, is observed in the tapered-vias. The vacancies in M2 are migrated to release the compressive stress at the corner of the fenced-vias, and the total number of vacancies in M2 is increased with increasing the M2 width, or essentially the total Cu volume in M2. Therefore, it is supposed that the voids at the corner of vias grow largely with increasing the M2 width, resulting in high failure rate of the fenced-vias in the wide M2.

To obtain the suitable via profile, we investigated the stress gradient as a function of taper angle θ of the vias (Fig. 7). The stress gradient along the horizontal direction at the via corner drastically decreases as the taper angle increases. This means that the stress at the via corner is improved by the tapered-vias. The tapered-vias (~105^{o}) provides higher thermal stability. The stress gradient along the vertical direction at the center bottom of via, however, has no significant dependence, suggesting that the via-taper control is not effective to suppress the voiding in M1 under the via. The other technique such as Cu alloying was utilized to eliminate the Cu voiding in M1 [4].

Based on these experiments, we applied this VF-MHM process to 65nm-node, 3 layered Cu DDI with a porous SiOCH low-k film (Fig. 8). The suitable profile of the tapered-vias with no fence was obtained to confirm the high thermal stability.

5. Conclusions

The tapered-vias improve the thermal stability of Low-k/Cu DDIs, as compared with the fenced-vias. The precise control of the via profile becomes very important to keep the via reliability for the 65nm nodes and beyond.

References

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[2] H. Ohtake et. al. *IEDM Tech. Dig.*, 2003, pp 853
[3] K. Higashi et. al. *Proc. IEEE IITC.*, 2002, pp 15.
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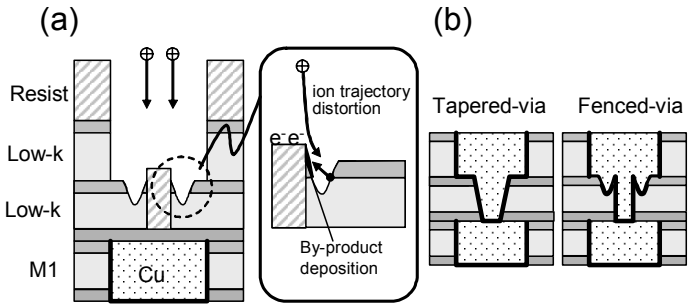

Fig. 1 Comparison between the tapered-vias and the fenced-vias; (a) the formation mechanism of fenced-vias by via-first resist-filling process, and (b) the profile difference between these vias in Cu-DDIs.

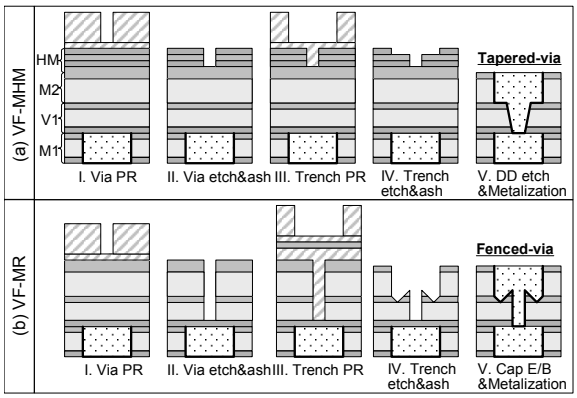

Fig. 2 DD formation flows; (a) via first multi-hard-mask (VF-MHM) process, and (b) via-first resist-filing (VF-MR) process. Tapered-vias are fabricated by MHM process, while the fenced-vias are obtained by MR.

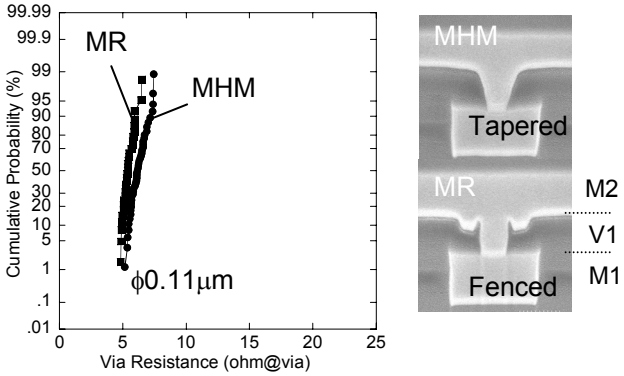

Fig. 3 Initial via resistances and SEM images of the via profiles in 10k via chain fabricated by VF-MHM or VF-MR.

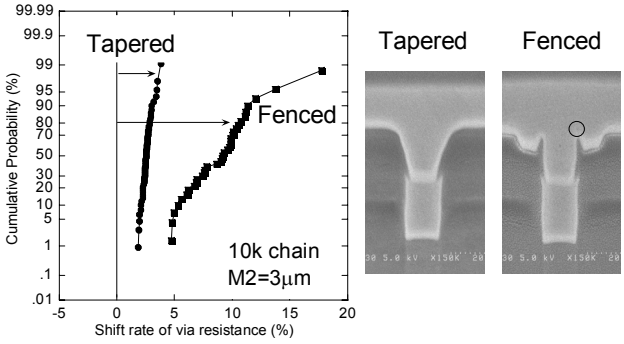

Fig. 4. Shift rates of the via resistance after 20 cycles of high-temperature T/C test (350 ºC, 30min). The FIB/SEM images are also shown after the test.

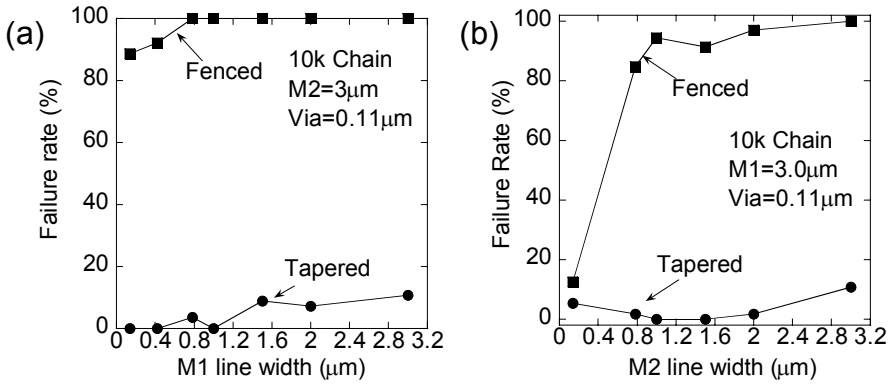

Fig. 5 Failure rates of the 10k via chain of the tapered- and the fenced-vias after the 20 cycles high temperature T/C test; (a) the dependence on the M1 width, and (b) the M2 width.

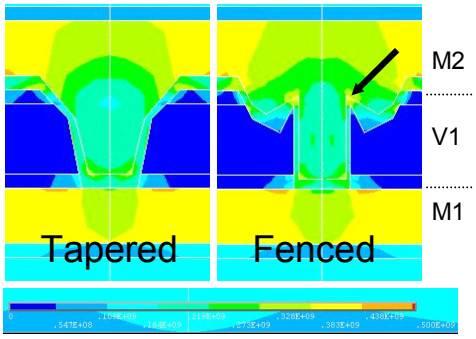

Fig. 6 Mises stress distributions in the Cu-DDIs. The stress is estimated by 3D finite element analysis at RT assuming the stress is free at the high temperature.

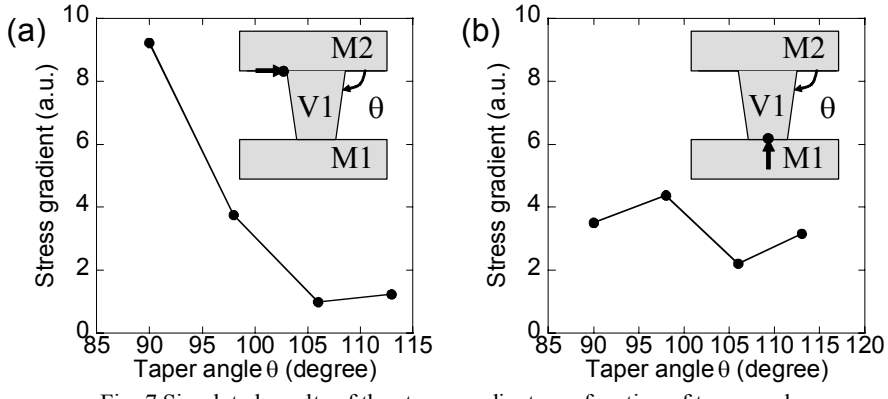

Fig. 7 Simulated results of the stress gradient as a function of taper angle;
(a) stress gradient along horizontal direction at the corner.
(b) stress gradient along vertical direction at the center-bottom of via.

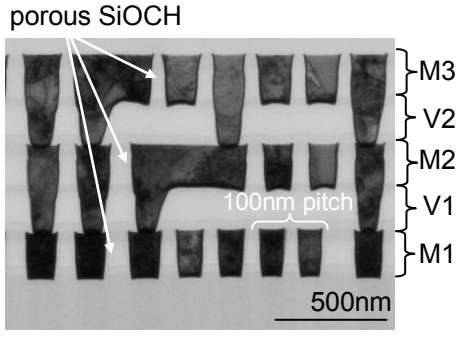

Fig. 8 TEM image of the 65nm-node, 3 layered Low-k/Cu DDI with the 0.1 μmϕ tapered-vias fabricated by VF-MHM process.