Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.900-901

C-8-1 (Invited)

Current Status and Forecast in High-Performance CMOS Device Technology

Toshihiro Sugii

Fujitsu Ltd., 50 Fuchigami, Akiruno, Tokyo 197-0833, Japan
Phone: +81-42-532-1253 E-mail: Sugii@jp.fujitsu.com

Introduction

Our high-performance planar bulk CMOS armed with aggressive process induced strain for 90/65nm node is reviewed from the point of on-current enhancing techniques. Through continuous efforts to increase on-current while scaling gate length, required targets for 90/65m node will be satisfied. For high-performance application at further nodes, a metal gates and enhanced stress control as well as conventional scaling must be introduced with least process complexity.

Scaling Issues in High-Performance CMOS Devices

The pace of scaling high-performance CMOS has slowed as can be seen in the recent ITRS roadmap. Main reason for this slowdown is reduced improvement in on-current with scaling transistors. There are three main causes. One is a delay in introduction of new annealing techniques, which results in a deeper extension junction and a high channel doping. The high doping in the channel reduces carrier mobility or carrier injection velocity at the source side of the channel. The high doping in the channel also increases sub-threshold slope, which results in degraded on-current under a constant off-current. The absence of a new, but matured annealing technique also does not improve lateral abruptness of an extension profile compared to the previous node, which prohibits the scaling in a gate to source/drain overlap length. The second cause for slowdown of scaling is that the scaling in electrical gate dielectric thickness has been delayed due to the difficulty in introduction of a very thin high-k dielectric and a metal gate with controlled work function. The third reason is that scaling threshold voltage is getting difficult from the point of static power consumption. Considering variation in threshold voltage, typical sub-threshold current should not be over several tens nA/μm.

Since we cannot expect higher on-current by scaling transistors because of above causes, a practical scenario toward high-performance should be rather conservative optimization and introduction of aggressive process induced strain.

90/65nm Technology

For high-end servers, we have developed high-performance CMOS devices through four stages as shown Figure 1. On stage I, CMOS technology with 40nm gate length was developed as a base flow in 2002[1]. On stage II, vertical scaling of the gate electrode and some process induced strain were introduced in 2003[2]. We optimized the process conditions for both a STI nitride liner and a contact etching stopper (CES)-SiN film to maximize the device performance. On stage III, short channel effects and mobility were improved by using a low temperature sidewall and optimizing gate oxynitride conditions[3]. On stage IV in 2004, enhanced process induced strain using a laminated CES-SiN was added[4]. Figure 2 shows Ion - Ioff relation of our n/pMOSFETs. A high drive current of 1120μA/μm for nMOSFETs and 690μA/μm for pMOSFETs at Ioff=100nA/μm is achieved. Figure 3 shows benchmarking of on-current and gate length under constant off-current of our nMOSFETs (stage I-IV) comparing with recent published high performance CMOS.

45nm and Further Node Technology

Figure 4 shows on-current, gate oxide thickness, and supply voltage data collected from major conferences. 2003 ITRS requirement for high performance transistors is also added. On-current was rapidly increased at around 0.18μm node. This is because the gate oxide thickness could be aggressively thinned and the supply voltage was large enough compared with the threshold voltage. But recent transistors with gate length of 40 to 50nm do not show much advance in on-current. This is because of scaling limitation in gate oxide thickness, shallow junction, and threshold voltage I mentioned before. From our data, we can keep pace with ITRS requirement until 2006.

After 2007, besides further improving process induced strain, a high-performance transistor needs some technology boosters to realize ITRS requirements. As well known, a high-k gate insulator and a metal gate are most important candidates. Different from transistors for low standby power application, a high-performance transistor needs aggressively scaled gate oxide thickness. Figure 5 shows the relation between electron mobility and EOT collected from major conferences[5]. From the figure, electron mobility decreases rapidly with scaling EOT. It seems to be difficult to apply a high-k gate insulator to a high-performance application where the EOT of less than 1nm and a high on-current are requisite. On the other hand, considering large permitted gate

leakage current and recent results on SiON[6], improved SiON gate insulator seems to be continuously used.

A metal gate is needed not only for a high-performance use but also for a low standby power use. To introduce a metal gate, there are three process candidates, a dual metal gate, a tunable metal gate like nitrogen-implanted Mo, and FUSI, a fully silicided gate. Less process complexity can be expected for FUSI process.

The most important issue related with the metal gate is the threshold voltage control. Figure 6 shows the recent results of Ni fully silicided gates[7]. Work function difference of 0.91 eV would be expected by segregation of dopants, suppression of dopant penetration, and adjusting composition of NiSix.

Conclusion

High-performance bulk CMOS technology is reviewed for 90/65nm node and is forecasted for further node from the point of on-current enhancing techniques.

References

1) S. Nakai et al., Symp. on VLSI Technology, Dig. Tech. Papers 2002, p.66

2) K. Goto et al., Symp. on VLSI Technology, Dig. Tech. Papers 2003, p.49

3) K. Goto et al., IEDM Tech. Dig. 2003, p.623

4) K. Goto et al., IEDM Tech. Dig. 2004, p.209

5) T. Sugii, Proc. VLSI Technology Short Cource 2004

6) D. Matsushita et al., Symp. on VLSI Technology, Dig. Tech. Papers 2004, p.172

7) K. Hosaka et al., Symp. on VLSI Technology, Dig. Tech. Papers 2005, p.66

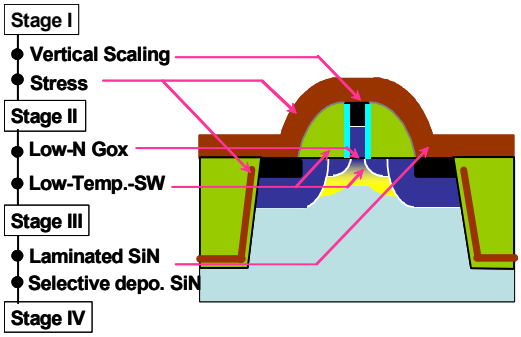

Fig.1 History of our HP-transistor development

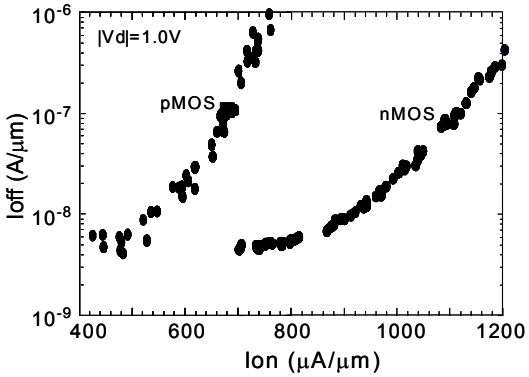

Fig.2 Ion-Ioff characteristics of Stage IV devices

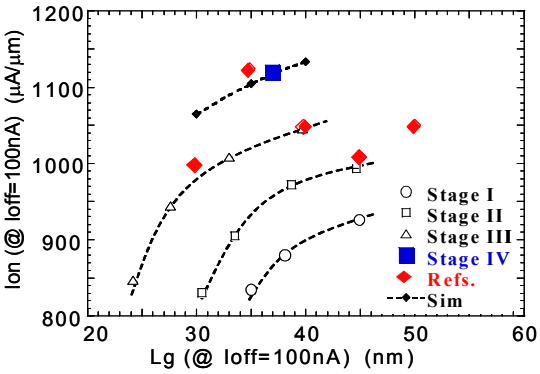

Fig.3 Benchmarking of Ion-Lg under constant Ioff

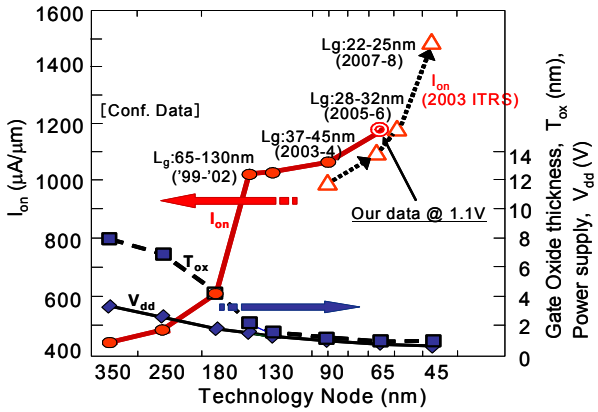

Fig.4 Ion,Tox, and Vdd collected from conferences

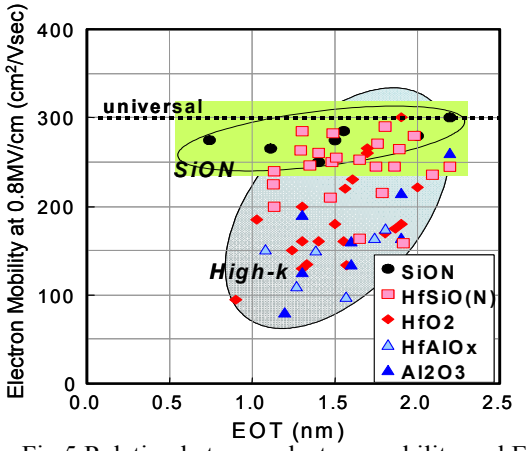

Fig.5 Relation between electron mobility and EOT

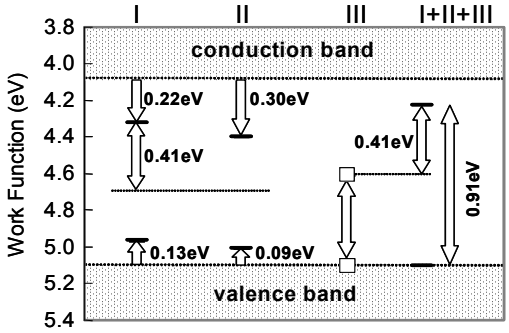

Fig.6 Work function control of NiSi-FUSI