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Buried Epitaxial, $Si_{1-y}C_y$ (y = 0.07 %) for the Suppression of Leakage in SPER (550 °C 10 mins) Activated Junctions and Current Drive Enhancement in *n*MOSFET

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Abstract

We demonstrate on the application of a buried epitaxial carbon, $Si_{1-y}C_y$:y = 0.07 %, of two functionalities: (i) to suppress S/D EOR defects under low temperature (550˚C 10 mins) SPER junctions (ii) as a diffusion barrier to boron diffusion in the channel region. The carbon devices display significantly suppressed junction leakage of higher than 2 orders with enhancement of 8 % in drive current, I_{on}:I_{off} of 2 orders and a reduction in body factor (3 times) in *n*MOSFETs. These changes in channel performances are consistently explained by the decrease in impurity concentration in the channel region (4 folds). Tradeoff however, is observed with the introduction of noise in junction capacitance and an increase in the EOT of the carbon device.

Introduction

Low temperature Solid Phase Epitaxy Regrowth (SPER) for annealing is gaining renewed interest [1] as the need for low thermal budget fabrication becomes mandatory to facilitate future scaling of MOSFETs. However, the secondary end-of-range (EOR) defects remain after SPER limits the application of the technique. Another crucial consideration is achieving highly abrupt and non-uniform channel profiles [2] for the suppression of short channel effects (SCE) which is compulsory with the scaling. Substitutional carbon in the silicon substrate on the other hand is known to act as sink for silicon interstitials which suppresses EOR defect formation [3] and efficient boron diffusion barriers [4]. In this work, a two-fold function of the manipulation of the silicon self-interstitial is demonstrated using the buried epitaxial carbon layers in order to: (i) effectively suppress the junction leakage cause by the EOR defects in the S/D region and (ii) as diffusion barrier to prevent enhanced diffusion of boron in the channel region which are consistently exposed to interstitial injection and high temperature steps.

Device Fabrication

The schematics (Fig. 1) of the fabricated *n*MOSFET, is shown with the buried epitaxial carbon, $Si_{1-y}C_y$ layer. While maintaining identical implantation conditions in the fabricated devices, variation is performed to the initial substrate with buried $Si_{1-y}C_y$ layer, and the *SiCap* thickness. The *SiCap* layer was intended to allow for good quality gate oxide formation, and to adjust the depth of the carbon layers. An as-implanted simulation was performed, shown in Fig. 2, to determine the respective arsenic damage profiles in the S/D regions (Fig. 2a) and boron profile in the channel region (Fig. 2b). It is worthwhile to note that EOR is only present from the S/D implants. Growth dimension of the *SiCap* and buried carbon layers are summarized in the table in Fig. 3 to overlap specific regions of the implantation profiles in the channel and S/D. The total grown epitaxial layers were maintained at 180 nm. The wafer *SiCap* = 180 nm only has epitaxial silicon, was used as the control.

The flow of the device fabrication is shown in Fig. 4. Epitaxial carbon layers were grown on *p*-type silicon (100) using LPCVD, where the substitutional carbon was determined to be 0.07 %. Channel punchthrough implant using boron, B^+ with a dose of $\times 10^{13}$ cm^{-2} range and BF_2^+ for the V_t implantation at 40 keV. RTO was grown at 950 ˚C for 30 s for gate insulator followed by an in-situ doped polysilicon gate, arsenic S/D extension implant, and spacer deposition. Deep source-drain arsenic implantation of dose 3×10^{15} cm^{-2} was performed at 70 keV for amorphization, followed by low temperature SPER annealing at 550 ˚C for 10 mins. Finally, nickel salicide was formed using RTA conditions at 400 ˚C for 30 s.

Junction Characteristics

Throughout the entire reverse biased voltage in Fig. 5, the control SPER device reveals significantly higher leakage current compared to the carbon devices of ~500 times. Between the carbon devices, there are less significant differences in the leakage features, indicating that the carbon incorporation solely at the EOR region was sufficient for the elimination majority of the leakage current component due to the implant defects. Although the leakage remains high compared to theoretical junction, there is a substantial decrease in the SPER devices. Fig. 6 reveals the evolution of noise in the junction capacitance, inherent larger overlapping region of the carbon layers. The arrows indicate the junction reverse bias voltage, V_{rev} for the observation of the noise. By reducing the overlap in the junction, the V_{rev} onset for the noise in capacitance measurement may be minimized shown in Fig. 7.

*n*MOSFET with $Si_{1-y}C_y$ Device Characteristics

The I_D-V_{GS} characteristic presented in Fig. 8 shows significant difference between the devices in the accumulation regions. GIDL effect is observed the carbon device whereas the characteristics are vastly different for the control silicon device, indicating a different junction leakage mode. The I_D-V_{DS} (Fig. 9) reveals enhancement in the overall current drive characteristics where improvement of 8 % compared to the control silicon is obtained. As the silicon capping layer increases from 20 nm to 90 nm, the current drive, is observed to decrease and plateaus eventually (Fig. 10). An explanation for the trend is the reduction of ionized impurity scattering in the active channel region with the buried carbon layers, supported by the reducing in V_t (Fig. 11) and decreasing acceptor concentration of (~4 folds) (Fig. 12) with carbon presence towards the channel regions. The I_{off} on the carbon devices depicted in Fig. 10 is significantly suppressed, in the range of two orders relative to the control. This reduced I_{off} results in remarkable increase in the I_{on}:I_{off} ratio shown in Fig. 11 in the carbon devices. The gate leakage measurement in Fig. 13 shows an overall reduction compared to the control of approximately two orders. The decrease is effectively caused by the increase in the EOT of the carbon devices, indicated by the decrease in the accumulation capacitance profile in Fig. 14. The V_t dependence on body biasing is shown in Fig. 15 where the carbon devices shows suppressed dependence on the body biasing effect. It was determined through capacitance simulation that this decrease in body factor correlates well with the extracted body doping concentration in Fig. 16 with increasing carbon presence towards the channel. This observation may be explained with the decrease to the boron diffusion profiles in the channel depletion with presence of carbon overlaps.

Conclusion

A strategic application of buried epitaxial carbon is demonstrated to concurrently suppress the junction leakage in SPER devices and enhance the drive current. The leakage suppression is attributed to the substantial elimination of EOR defects and body effect suppression with current drive enhancement with the modification to the boron profile in the channel with the varying carbon presence.

Acknowledgements

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References

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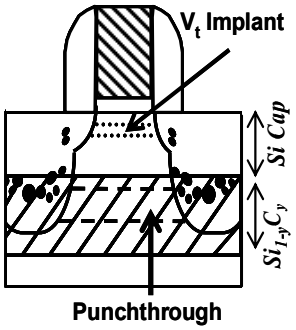

Fig. 1: Schematic illustrates the buried carbon layer grown relative to the implanted profiles in the channel and S/D regions. Solid dots represents in implantation defects.

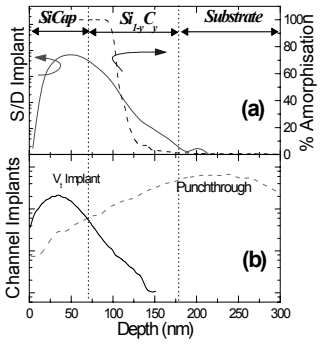

Fig. 2: Simulation of the implantations performed in the (a) S/D and (b) channel regions. EOR only present in the S/D implants, indicated by amorphization transition.

SiCap	$Si_{1-y}C_y$	Regions of Carbon Overlap
20	160	S/D EOR + S/DE EOR + Punchthrough + Vt
60	120	S/D EOR + Punchthrough + Vt
90	90	S/D EOR + Punchthrough
180	0	(Control) None

Fig 3: Table representing the dimensions for the buried epitaxial carbon layers and SiCap, overlapping specific implantation regions in the S/D and channel respectively.

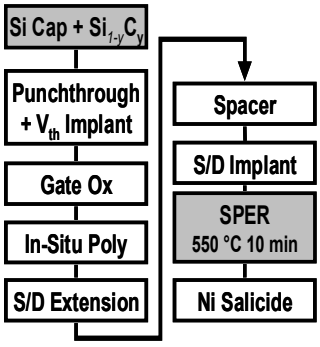

Fig. 4: Flowchart shows the process flow for device fabrication. Highlighted boxes show the main modification to the fabrication.

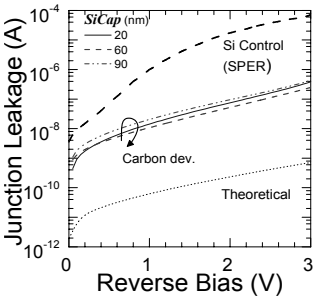

Fig. 5: Junction leakage of the carbon devices show significant suppression in the junction leakage compared to the control device.

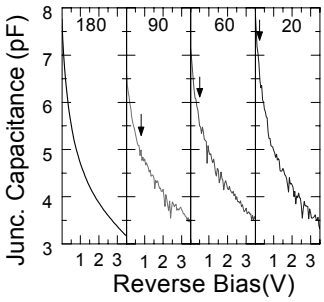

Fig. 6: Evolution of the noise in the capacitance measurements with increasing carbon overlap with the junction.

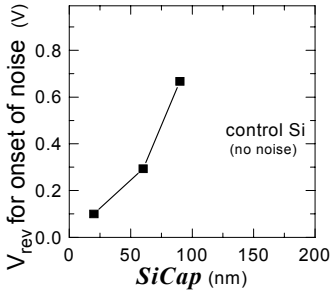

Fig. 7: The reverse bias, V_{rev} for the onset of the junction capacitance noise features increases with ***SiCap***. No noise seen in control.

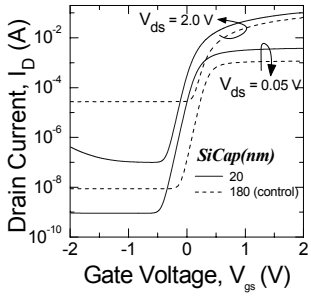

Fig. 8: I_D-V_{GS} comparing the device with 20 nm capping layer and the control. Carbon device indicated lower I_{off} and higher drive current

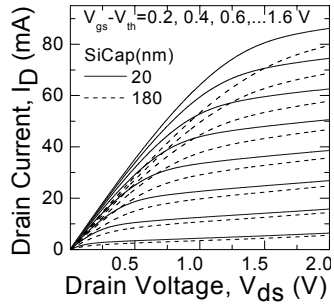

Fig. 9: I_D-V_{DS} of the 2 devices with higher drive current on the carbon device, with an 8% enhancement.

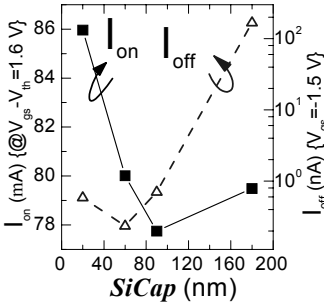

Fig. 10: Drive current of the devices decreases with increasing ***SiCap***; eventually plateaus.

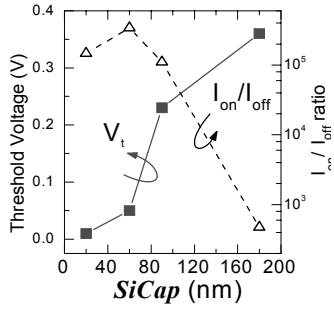

Fig. 11: V_t decreases with decreasing, ***SiCap***; suggesting reduced impurity at the channel.

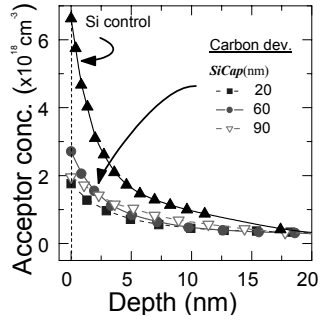

Fig. 12: Extracted doping profile indicated an increase by 4 folds in the channel of the control device

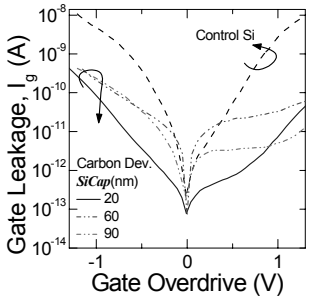

Fig. 13: Gate leakage of the carbon devices displays reduced gate current to 2 orders.

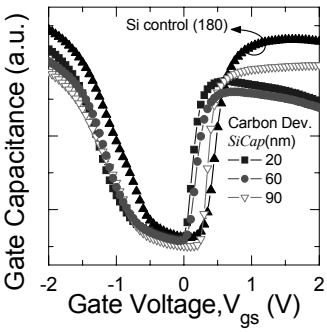

Fig. 14: Gate Capacitance of the fabricated device.

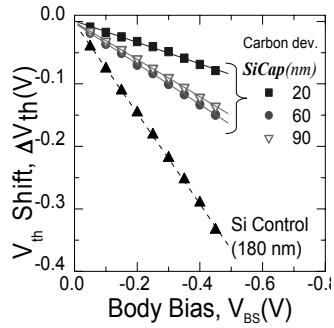

Fig. 15: Control silicon showed highest dependence of ΔV_{th} on increasing body biasing

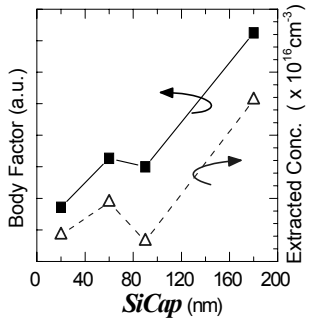

Fig. 16: Extracted body factor correlates with the body concentration in the active channel