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Integration of ultra shallow junctions in PVD TaN nMOS transistors with Flash Lamp Annealing

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Abstract

We demonstrate that the use of Flash annealing to achieve ultra shallow junctions leads to strong suppression of the Short Channel Effects (SCE) without compromising device performance in PVD TaN nMOS transistors. We show that a deep Ge implantation at the gate edges can be an excellent solution for further improvement in the B halo activation. The junction overlap length, the S\D resistance and the device performance are found to be dependent on the defects evolution as a function of the Flash peak temperature.

Introduction

Ultra shallow and abrupt junctions are one of the major requirements for further scaling of planar CMOS transistors. Several techniques such as low temperature processing [1], and high temperature Flash annealing [2], [3] have demonstrated great potential for improving the junction profiles and for increasing the dopant activation above the solid solubility equilibrium limit. However, many integration problems both in pMOS [4] and nMOS transistors have prevented an extensive use of these advanced techniques

We investigate the integration of PVD TaN nMOS transistors with 25nm depth diffusion-less junctions targeting 45nm gate length. A deep amorphous layer is created at the gate edges to improve the halo activation and to move away the End Of Range (EOR) defects region from the extension junction depletion region. We studied the defects evolution as a function of the Flash peak temperature and during post annealing both in the EOR and in the junction overlap region. The impact of the Flash peak temperature on the defects and on the transistors characteristics is investigated.

Experimental

The transistors are processed (Fig. 1) with a standard Shallow Trench Isolation (STI) module. The gate stack consists of 1.4nm SiON, 17nm PVD TaN and 100 nm of poly silicon. A metal gate electrode eliminates problem with poly depletion due to insufficient diffusion of dopants. The suitability of PVD TaN on 1.4nm SiON has already been demonstrated [5]. B halo implantation with the same dose is performed on all the wafers. A low dose Ge implantation allows for a deep amorphous layer formation before the As extension junction implantation. A low temperature spacer is formed without re-growing the amorphous Si layer. The Flash lamp annealing tool used for the junctions doping activation is 3000 times faster in ramp up and ramp down than the conventional Spike RTA annealing. The chamber reaches an intermediate temperature of 700^{o}C (iRTA) before ramping up to a Flash peak temperature (fRTA) of maximum 1300^{o}C for few milliseconds. The a-Si region created during the As and Ge implantations re-crystallizes during the iRTA and the doping is activated. NiSi completes the FEOL process.

Results and Discussion

After Silicon re-crystallization at 700^{o}C, we observe the formation of defects (stacking faults of micro-twins) in the junction to gate overlap region, as shown in Fig. 2. The stress induced during the re-growth between the S/D amorphous region and the c-Si under the gate creates a plane mismatch. Nevertheless, based on the electrical characterization data presented in this paper, these defects vanish at the interface after the fRTA at 1300^{o}C.

The SIMS As junction profiles implemented in the nMOS transistors are shown in Fig. 3. The junction depth does not significantly change with increasing Flash peak temperature. At 1300^{o}C fRTA the As diffuses towards the Si interface. Furthermore a shoulder at a concentration of 5E20 cm^{-3}, not present in the SIMS profile for lower temperature annealing, indicates a high doping activation. In fact, despite an unchanged junction depth, the sheet resistance drops as a function of the fRTA, as shown in Fig. 4.

In Fig. 5, we analyze the stability of the Flash annealed junctions as a function of post annealing temperature in a range between 600^{o}C and 950^{o}C. The junction sheet resistance degrades starting from a temperature of 750^{o}C even for the junction annealed with the highest 1300^{o}C Flash peak temperature. This demonstrates that the high As doping activation is meta-stable. The defects in the junction depletion region increase the junction leakage, as shown in Fig. 6. The leakage, measured directly in transistors, is controlled by the deep S/D junction with a much larger area compared to the shallow extension junction. At 1100^{o}C the junction leakage further increases compared to 700^{o}C as the B doping reaches higher activation. Due to a partial dissolution of the defects, the leakage drops by more than one order of magnitude at 1300^{o}C.

The deep Ge pre-amorphization at the gate edges provides high meta-stable B halo activation to occur during the re-growth of the a-Si layer. Therefore, even with low temperature annealing, a good Vt control down to 50nm gate length devices is obtained, as shown in Fig. 7. A high Flash peak temperature further increases the B halo doping activation allowing for a significant improvement in SCE over the spike reference devices. Nevertheless Fig. 8 reveals that the device performance depends on the Flash peak temperature. As a consequence of the defects located in the junction to gate overlap region, the overlap resistance strongly increases. High Flash peak temperature solves this problem allowing for As doping re-activation while dissolving the defects at the interface. At a fixed off state current of 0.1nA, the device performance is equal for Flash and spike annealed transistors but the Lmin reduces by 50nm with Flash annealing, as shown in Fig 9. The overlap length significantly decreases for Flash anneal, as shown in Fig. 10. Furthermore for higher Flash peak temperature the overlap length increases. This is a confirmation of what was explained above. The S\D resistance extraction, presented in Fig. 11, enlightens an improvement going towards high Flash peak temperature when the overlap length increases. A further analysis of the off state gate current (Fig. 12) shows a current decrease for the Flash annealed devices over the spike ones related to a reduced overlap length.

Conclusion

We have demonstrated that Flash annealing can lead to considerable reduction in SCE without degradation in Ion. A deep amorphous layer at the gate edges allows for high doping activation. The defects introduced during the implantation and during the re-growth can be removed by high temperature Flash annealing. The overlap and S/D junctions resistance as well as the transistors performance also improves with increased Flash peak temperature.

References

[1]R. Lindsay et al., IJWT 2004, [2]T. Ito et al., VLSI Tech. Dig. 2003, [3]A. Satta et al. , MRS 2004, [4]S. Severi et al., IEDM Tech. Dig.2004, [5]K. Henson et al., IEDM 2004, [6]S.Severi et al., ESSDERC 2004

- STI isolation +V_T-adjust (Boron)
- Gate stack:
  - 1.4nm SiON
  - 17nm TaN deposited by PVD
  - 100nm polysilicon
  - 193nm litho + gate etch
- Boron pockets implant
- Germanium pre-amorphization (optional)
- Extension implant As 5keV 1e15cm^{-2}
- Spacer (400 °C) + As deep S/D implant
- Flash annealing
- NiSi formation on S/D areas and gate

Fig. 1 Process flow for the PVD TaN gated transistors with Flash annealing.

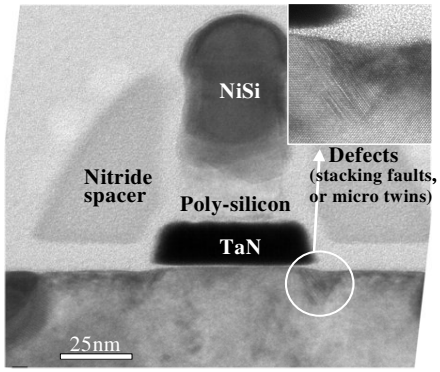

Fig. 2 TEM picture of metal gate nMOS transistors annealed at 700°C with Ge implantation.

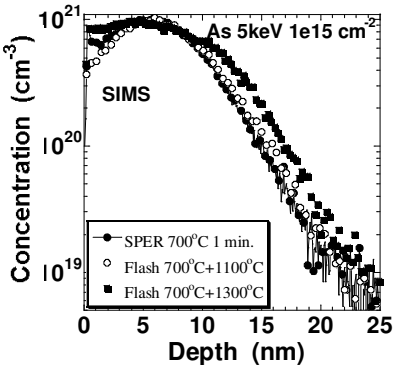

Fig. 3 SIMS profiles of As 5keV 1e15 cm^{-2} for different Flash annealing temperatures.

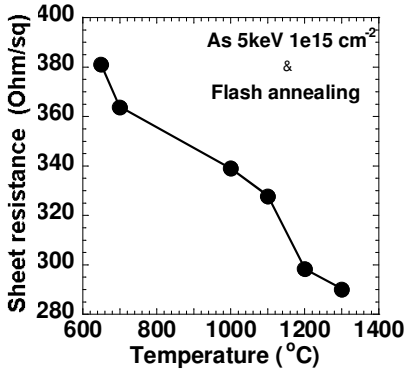

Fig. 4 Sheet resistance versus Flash peak temperature.

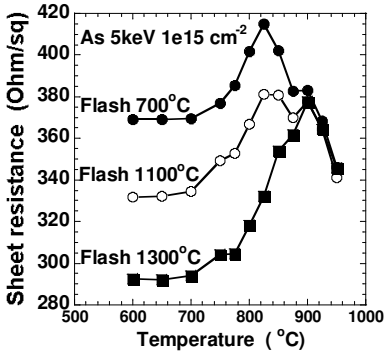

Fig. 5 Sheet resistance of Flash annealed junctions after post annealing for 1 minutes.

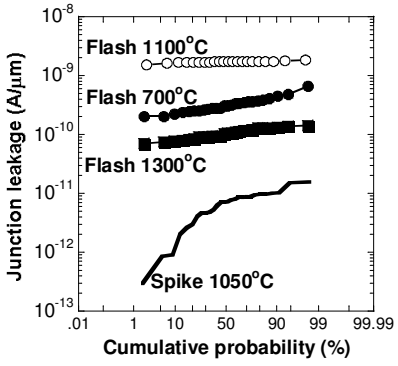

Fig. 6 Junction leakage measured on transistors with Vd=1V. B pockets are implanted.

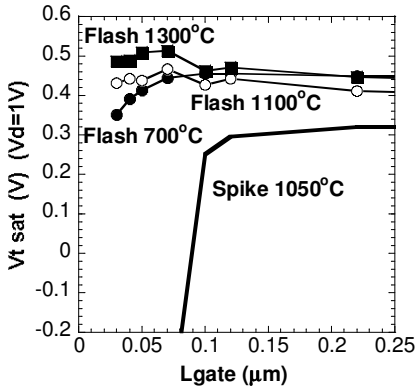

Fig. 7 Vt sat. measured at Vd=1V for nMOS transistors with Flash or spike RTA annealing.

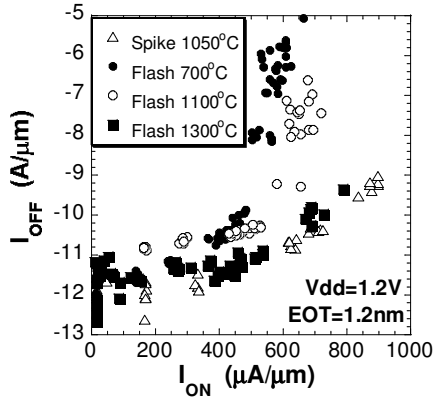

Fig. 8 Performance of nMOS transistors after Flash annealing at different temperatures.

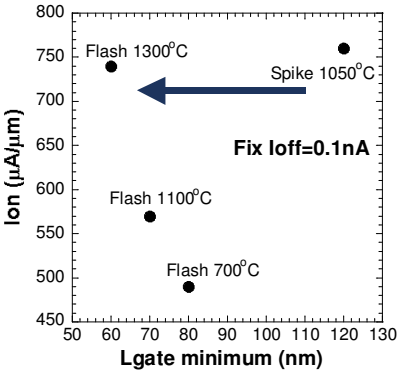

Fig. 9 Ion versus L_{MIN} for different Flash annealing temperature

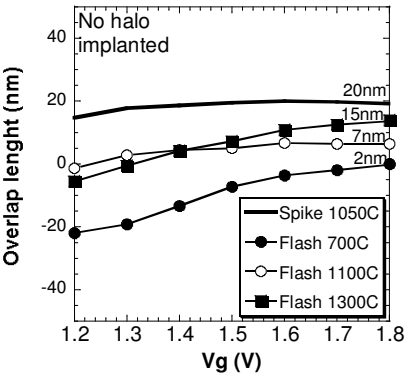

Fig. 10 Junction overlap lengths extracted from I_B in inversion versus L_{POLY}

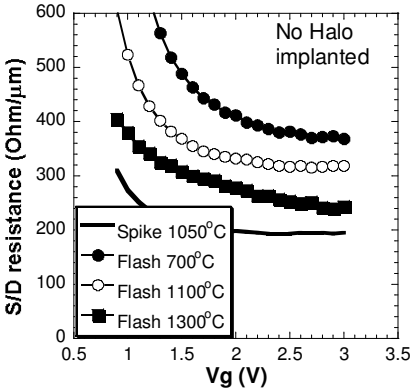

Fig. 11 S/D junctions resistances extracted from R_{TOT} versus L_{EFF} for small L_{GATE}.

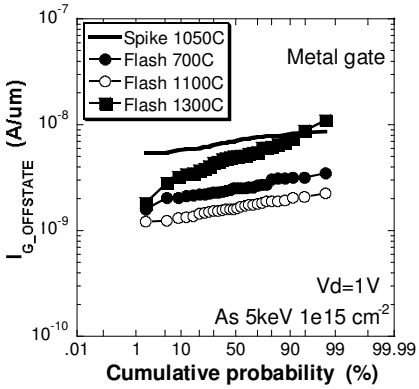

Fig. 12 Gate overlap currents for equal junction implant and different Flash temperature.