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Ultra Shallow Junction Formation Using Plasma Doping and Laser Annealing for Sub-65 nm Technology Nodes

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Abstract

Plasma doping and laser annealing are successfully integrated into the conventional p-MOSFET process to form an ultra shallow junction (USJ). Comparing with the conventional combination of ion implantations and rapid thermal annealing (RTA), junction depth (X_J) and sheet resistance (R_S) are reduced. Also, significant improvement of the short channel effect without the degradation of on-current is observed.

Introduction

As the design rule of device is scaled down, the SCE such as V_{TH} roll-off and drain induced barrier lowering (DIBL) increases. To reduce the SCE, source/drain junction depth should be reduced, but this will lead to increased series resistance. Therefore, technologies to achieve high activation rate in low thermal budget condition are demanded. The conventional techniques such as beam-line implantation and RTA approach the practical and technological limit in sub-50-nm gate-length CMOSFET. In conventional USJ implantation, the low energy implantation (LEI) process has very difficult points to be overcome such as poor beam current and dopant self scattering effect. Therefore, plasma doping was introduced for USJ.

On the other hand, USJ can be made by using conventional LEI process, the junction depth would be increased during the following thermal process, especially for p-FET, due to the high diffusivity of boron and transient enhanced diffusion [1]. Therefore, there have been many researches to cope this problem with SPER, flash annealing, and laser annealing. However, they usually have resulted in the degradation of on-current due to increased parasitic resistance. Laser annealing is a promising technique to overcome this problem, because it has high activation energy and ultra-fast thermal process (<1 ms). Here, we propose a combined process of plasma doping and laser annealing for p-FET integration to solve the above problems.

Experimental

Figure 1 shows our MOSFET process flow. Key features are the gate oxide with plasma nitridation to prevent boron penetration and gate pre-doping using boron implantation to P-FET to reduce gate depletion. In the case of laser annealing, offset spacer was skipped because of little lateral diffusion. For SDE doping, plasma doping with BF_3, 600 V or 1 kV, and LEI with BF_2 (2 keV) were used. For activation process, spike RTA with the peak-temperature of 1050 ^oC and laser annealing with the temperature of about 1350 ^oC, where the annealing time is less than 1 ms, were carried out. Figure 2 shows the cross-sectional TEM image of a sub 50-nm gate length P-FET. In addition to the MOSFET fabrication, blank wafer test was performed to investigate the junction depth and sheet resistance using SIMS and 4 point probe.

Results and discussion

As shown in Fig. 3, the X_J-R_S plot exhibits that the plasma doping process has a good ability to reduce the junction depth, and laser annealing is found to be a better activation process than spike RTA and flash annealing. As shown in Fig. 4 of I_{ON}-I_{OFF} characteristics, plasma doping process gives better performance. This is because of the SCE improvement with plasma doping as shown in Fig. 5 (V_{TH} vs. L_{GATE}) and Fig. 6 (DIBL vs. L_{GATE}). Figure 7 and 8 shows the gate oxide QBD (charge-to-breakdown) and the gate oxide leakage current, with very small difference in between plasma doping and conventional ion implantation. Figure 9 shows I_{ON}-I_{OFF} characteristics of spike RTA vs. laser annealing with the plasma doping. In the case of laser annealing process, it shows remarkable reduction of off-state current. By the same reason, V_{TH} roll-off and DIBL are improved with laser annealing (Fig. 10 and Fig. 11).

On concern with the junction leakage, most previous reports represents that the laser annealing shows worse characteristics than spike RTA, but in our result, laser annealing after plasma doping is rather better (Fig. 12) [2, 3]. Because junction leakage is associated with doping concentration and defect density in depletion region, the result in Fig. 12 shows that the plasma doping is a less damage causing process and the laser annealing has a good defect curing ability, since the laser annealing process induces the same or higher doping concentration than spike RTA. As shown in Fig. 13, although the laser annealing is able to achieve high activation, inversion capacitance is degraded since it is a diffusion-less process. To reduce the poly depletion, additional thermal budget before SDE formation is required. Figure 14 shows that the large portion of the off-state current is the leakage of gate to source/drain overlap region, and the laser annealing has a merit in that sense. Figure 15 indicates that the shallower junctions we want, the higher temperature process we need such as laser annealing.

Conclusions

We have fabricated USJ devices with plasma doping and laser annealing. In the case of using plasma doping, the short channel effect such as V_{TH} roll-off and DIBL characteristics is improved by junction depth decrease. With the laser annealing, parasitic junction resistance is reduced because it is a diffusion-less activation process. We suggest that the combination of plasma doping and laser annealing be a good candidate for next generation junction technology.

Acknowledgement

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References

[1] S. C. Jain et al., J. Appl. Phy., Vol. 91, No. 11, p. 8919, 2002.
[2] Akio Shima et al., Symp. on VLSI Tech., p.174, 2004.
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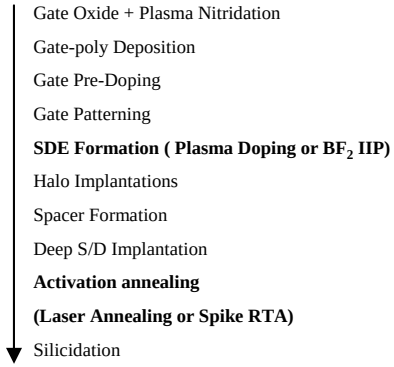

Fig. 1. Process flow of transistor fabrication using plasma doping and laser annealing.

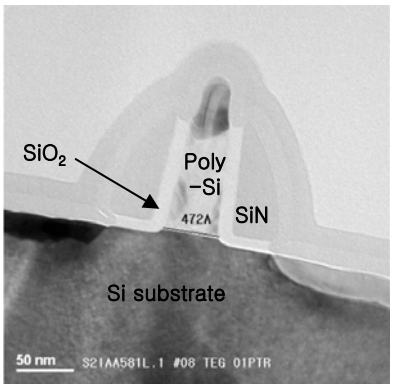

Fig. 2. Cross sectional TEM image of sub 50 nm gate length PMOSFET.

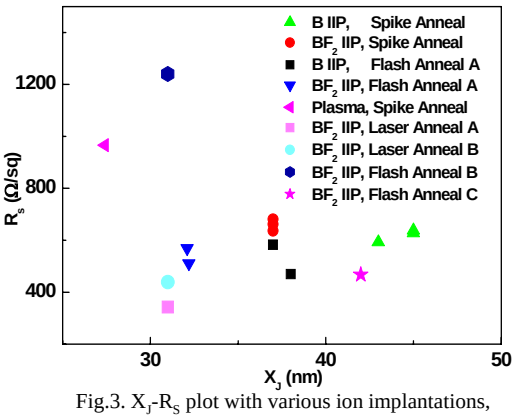

Fig.3. X_J-R_S plot with various ion implantations, plasma doping, and annealing processes.

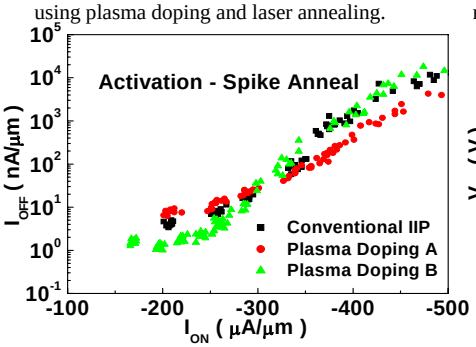

Fig. 4. I_{ON}-I_{OFF} correlation of conventional ion implantation and plasma doping.

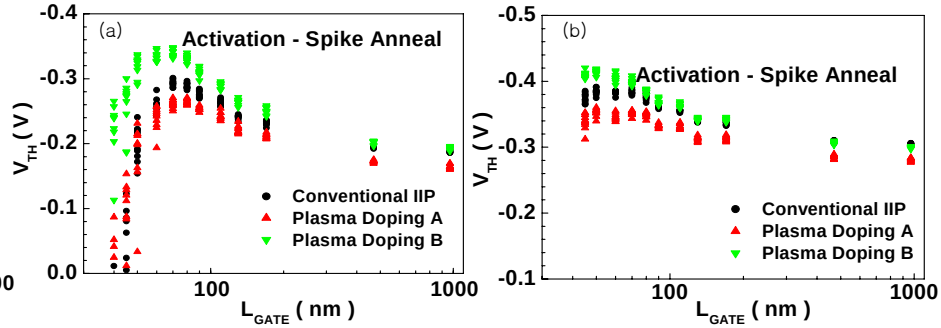

Fig. 5. (a) Low V_{TH} PMOSFET V_{TH} roll-off and (b) High V_{TH} PMOSFET V_{TH} roll-off comparision of conventional ion implantation with plasma doping.

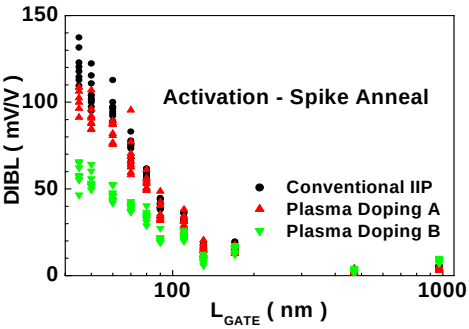

Fig. 6. DIBL characteristics of plasma doping and conventional ion implantation.

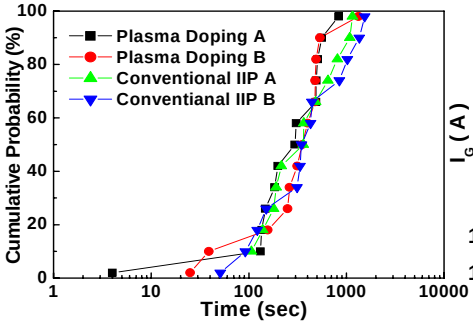

Fig. 7. Gate oxide QBD distributions of plasma doping and conventional ion implantation process.

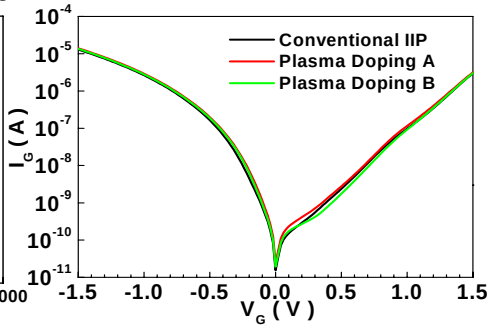

Fig. 8. Gate oxide leakage current characteristics of ion implantation and plasma doping process.

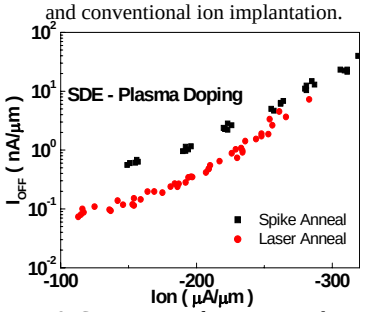

Fig. 9. Comparison of I_{ON}-I_{OFF} correlation of laser annealing with conventional RTA.

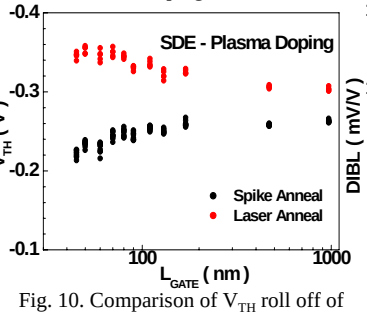

Fig. 10. Comparison of V_{TH} roll off of laser annealing with conventional RTA.

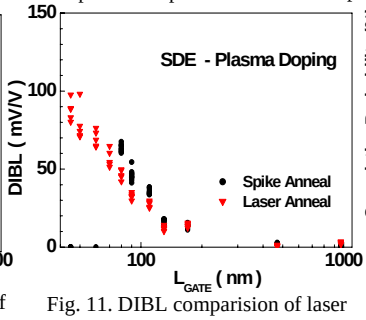

Fig. 11. DIBL comparision of laser annealing with conventional RTA.

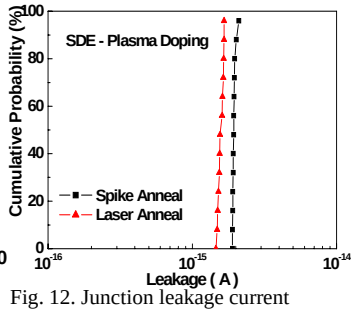

Fig. 12. Junction leakage current distribution of laser annealing and conventional RTA.

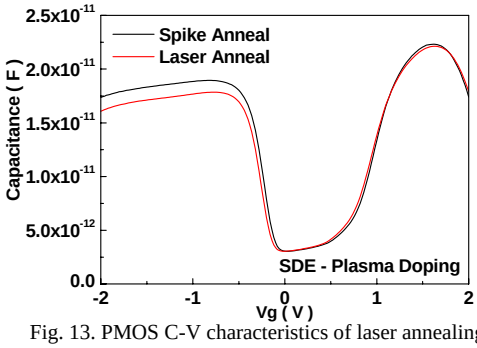

Fig. 13. PMOS C-V characteristics of laser annealing vs. conventional RTA.

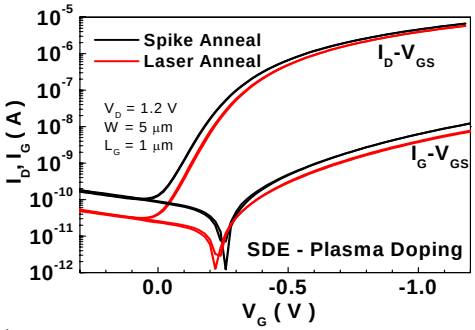

Fig. 14. I_D-V_{GS}, I_G-V_{GS} plot of laser annealing and spike annealing. L_{GATE}=1.0 μm.

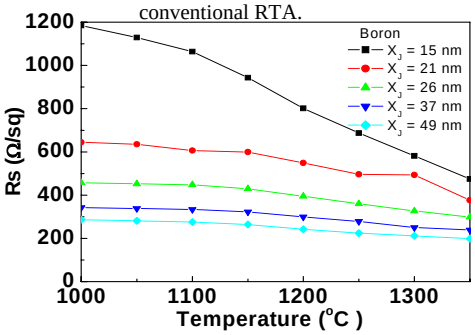

Fig. 15. Calculated plot of R_S vs. temperature of diffusion-less annealing process .