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The High Voltage Anti-Trend

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1. Low Potential for Low Voltage

Low voltage design gets considerable attention at technical conferences and in the technical press, but these days, the "real action" in analog circuit design is elsewhere. There are several reasons for this.

- The problems faced by designers in low voltage applications are not fundamentally different than what they have been dealing with for about a decade. Leakages are worse, headroom is tighter, flicker noise is ugly, but fundamentally, these are problems designers have been struggling with all along. Moreover, the techniques developed for the 0.35um generation are proving surprisingly resilient as each new process generation is encountered.
- Digital designers may actually be having more problems with the low voltage technologies than the analog designers. Consequently, standard processes often include enhancements like dual oxides, multiple thresholds, high voltage I/O devices, etc. that make life easier for analog designers as well.
- Analog on a really low voltage process is often not a good idea. Analog circuits interface with the real world, and real world voltages are not changing. More importantly, mask costs for the small geometries are escalating at an exponential rate. It becomes considerably less attractive to integrate analog on such an expensive process unless there is a clear advantage.

In contrast, high voltage applications are growing on a daily basis. Power management circuits, for example, are one of the fastest growing market segments in the analog semiconductor industry.[1] The trend toward integration continues unabated in the analog world with the important distinction that the current environment favors the integration of peripheral, interface and power supply circuits rather than the main signal processing blocks. Sensors and displays are an ever increasing part of electronic assemblies and many of these require voltages substantially outside the range of normal digital supplies. CCD clock lines, LCD drive signals, and speaker inputs all require supplies as high as 15 volts. With the recent emphasis on portability, sophisticated power management techniques are required to extend battery life and mitigate thermal issues resulting from small, tightly packed equipment casings. This means high efficiency regulators and DC-DC converters that must work with external supplies, and withstand kick-back, load dumps, generator spikes and general mishandling.

A typical application is shown in Figure 1. This monolithic system handles power management and a host of supervisory functions for CDMA handsets. [2] 15 voltage regulators, Li ion battery charger, real time clock, keypad interface, power supply sequencing control and a variety of other functions are integrated. Although the nominal battery voltage is only 3.6 volts, the battery charger must deal with a 12v supply if an automotive adapter is used. Thus both high voltage capability, and dense low voltage logic are required.

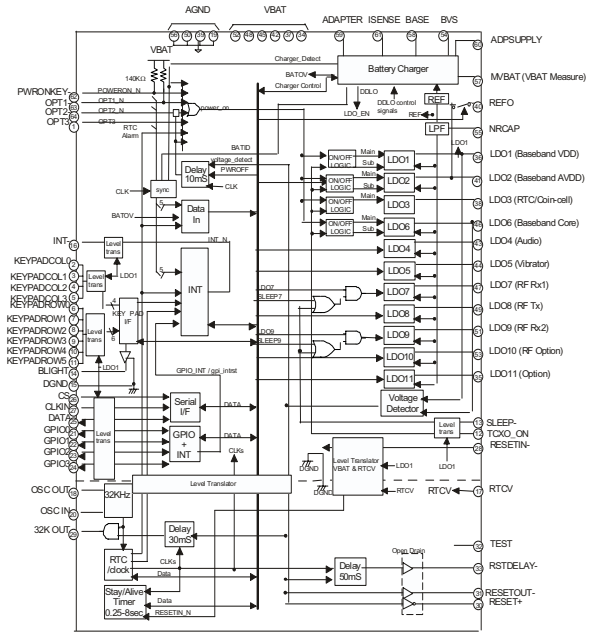

Fig. 1 Typical Cell Phone ASIC.

2. Process Implications

All of these new -or newly integrated- applications conspire to create commercial pressure for higher, rather than lower, voltage. The demand for voltage handling capability has sparked a quiet revolution in the semiconductor industry. Many foundries now offer specially adapted processes with voltage capability up to 50 volts. Originally, high voltage devices took the form of bipolar transistors and thick oxide MOS devices that were minor extensions of older digital processes. Now however lateral DMOS devices are common. In the DMOS transistor, the high drain voltage is dropped across a large drain depletion region, so a thin gate oxide can be used and high transconductance maintained. Although it cannot be safely done by the process user, scaling the devices to handle different voltages is a

relatively straightforward process of scaling the drain depletion region.

Since the DMOS is compatible with conventional CMOS, a variety of system blocks can be integrated with the power devices. Some manufacturers offer multiple well options that allow for full isolation of both N and P channel DMOS transistors. Such isolation is particularly useful when the circuit must handle voltages outside its own supply range, as in the case of charge pumps. An additional benefit of the well isolation is that it also serves to insulate the huge transients of the power device from the delicate low-voltage peripheral circuitry and signal processing on the chip.

The thin gate oxide of the high transconductance DMOS transistor needs to be protected from over-stress during operation. This places a somewhat cumbersome burden on the circuit designer unless a zener diode of the correct voltage is available to limit the gate excursions.

3. Circuit Implications

High voltage and power devices require a completely different set of circuit architectures than most analog designers are familiar with. In the majority of applications, the high voltage device is used as a switch. This applies naturally to power management applications and motor drives, but also to signal chain components like class-D amplifiers.

When a power switch is off, of course, it dissipates no power. When it is fully on, the voltage drop across its terminals should be low, so that even though it is conducting current, the dissipation is low. Low switch dissipation is important for die temperature considerations but also for the efficiency of the overall system, since only the power consumed in the load is useful.

The critical problem for the circuit designer is how to turn the power devices on hard (for minimum resistance) and fully off in a short amount of time. Time spent in the transition region is wasteful, because the device is partially on and resistive. Slow, weak drive will not only lower the efficiency of a switching circuit, but because of device self-heating, switch resistance can increase leading to thermal runaway and permanent transistor failure. For reasons of interface convenience, circuit density and power dissipation, the control circuitry is always built with small, low voltage transistors. This obliges the designer to come up with drivers and level shift circuits that translate logic level signals into crisp, reliable waveforms that quickly turn the device on as hard as possible without exceeding the maximum voltage that the control terminal, such as the gate of a DMOS device, can withstand. This is further complicated by the fact that one of the devices (usually the P-channel DMOS) must be driven relative to a high voltage supply not shared by the low voltage circuitry.

Generally the output power devices are big and represent a significant load in their own right. To achieve rapid switching, driver circuitry must source or sink a considerable amount of current to change the output state. But running the driver circuits at high quiescent currents again wastes valuable milliwatts. This leads to the further design challenge of how to drive the output transistors without using too much power: How to "drive the drivers".

One interesting solution is presented in Figure 2. [3] (The full system, describing the integration of low voltage ΔΣ modulators along with the power devices can be found in reference [4].) Here a large NDMOS device is pulsed on momentarily to pull a large current from the gate of the output PDMOS driver and turn it on quickly. A zener diode limits the gate swing of the PDMOS, preventing any damage. Once the large NDMOS device is turned off, a tiny "trickle current" is supplied by a much smaller NDMOS to keep the gate of the PDMOS driver from drifting back up to the positive supply rail. (A separate circuit is required to turn the PDMOS off efficiently.)

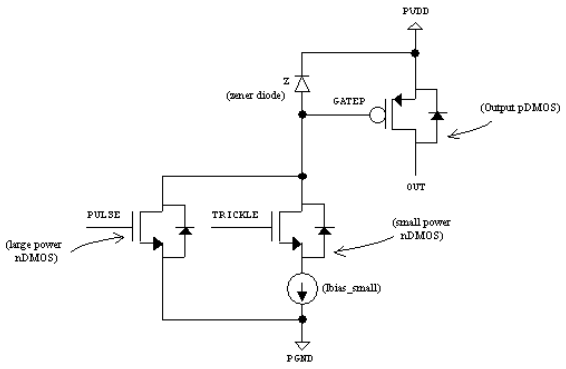

Figure 2. High-side DMOS switch driver.

4. The Future

Although not as publicized as the low voltage analog designs, high voltage analog ICs are an important –if not dominant- commercial reality. Foundries have already begun competing to offer the lowest resistance switches integrated with the finest geometry CMOS. Young analog designers entering the field may be surprised that their first job is not coaxing millivolts of headroom out of a low voltage opamp, but fending off tens of volts from a hostile inductive load. It is a brave new world, with lots of interesting new challenges.

References

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[4] E. Gaalaas, B. Liu, and N. Nishimura, "Integrated Stereo ΔΣ Class D Amplifier", *2005 IEEE International Solid-State CircuitsConference,* Paper 6.6.