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A New Protection Circuit for improving Short-Circuit Withstanding Capability of Lateral Emitter Switched Thyristor (LEST)

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1. Introduction

MOS-gated thyristors such as MOS-controlled thyristor (MCT), base resistance controlled thyristor (BRT) and emitter switched thyristor (EST) may be attractive for high power applications because of the lower forward voltage drop than that of insulated gate bipolar transistor (IGBT) [1]. The lateral MOS-gated thyristors have also attracted considerable attention for integration with CMOS in Power ICs [2-3]. Among them, the lateral EST (LEST), of which cross-sectional view is shown in Fig. 1, may be promising due to its unique gate-control current saturation characteristics, which can ensure a wide safe operating area (SOA) [4]. However, the current saturation of the LEST is severely limited by the breakdown of the lateral MOSFET, which occurs because the floating n+ voltage follows the increasing anode voltage during normal thyristor operation [5] and thus, the LEST may not exhibit high voltage current saturation.

The purpose of our work is to propose and fabricate a new protection circuit of the LEST, which allows a high voltage current saturation even at high gate biases without any sacrifice of the forward voltage drop without complex fabrication process. In order to verify the high voltage current saturation feature, 200 V LEST and protection circuit are fabricated on-chip integration by using an IGBT compatible 7-mask process. Our experimental results successfully show the operation of the hard switching fault (HSF) protection under the short-circuit condition.

2. Operation Principle of Protection Circuit

The cross-sectional view of a conventional LEST with the proposed protection circuit is shown in Fig. 1. The design parameters of fabricated LEST are summarized in Table I. The resistor R_G was deposited with 3500 Å thick LPCVD polysilicon and the protecting MOSFET M_P was fabricated in the p-base region without any additional p-well process step.

When the floating n+ voltage (G_P) is larger than the threshold voltage of the protecting MOSFET M_P, the inner gate voltage (D_P) is decreased according to the resistance ratio between R_G and the on-resistance of M_P. Because the LEST carries the thyristor current in series through the lateral MOSFET, the reduced inner gate voltage decreases the anode current. Note that NPN and PNP transistors in the thyristor begin to move out of the saturation mode when the anode current reduces. Until NPN and PNP transistors recover from the saturation mode and move to the forward active mode, the floating n+ voltage increases and thus, decreases the inner gate voltage and the anode current again. As a result, the transistors recover faster. This mechanism may be a positive feedback, which alters the thyristor operation mode from regenerative one to non-regenerative one when the floating n+ voltage does not exceed the breakdown voltage of the lateral MOSFET during the recovery. When the thyristor operates in the non-regenerative mode, the anode voltage can be supported by the junction between p-base and n-drift in Fig. 1, and the floating n+ voltage does not follow the increasing anode voltage. Therefore, high voltage current saturation can be achieved [6].

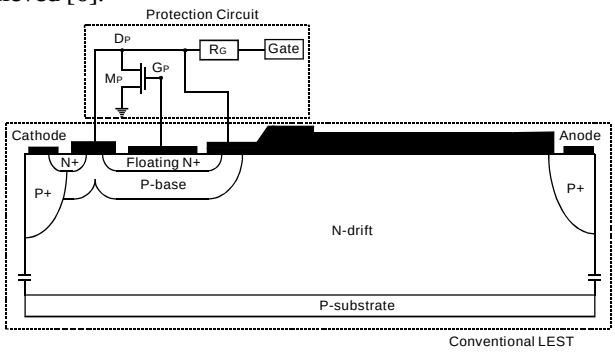

Fig. 1 Cross-sectional view of the conventional LEST with the proposed protection circuit

Table I. The design parameters of LEST with the protection circuit.

Design parameters		Value (Units)
Gate oxide thickness		1000 (Å)
Gate length		3 (μm) , 10 (μm)
Junction depth	N+cathode	1 (μm)
	P-base	3 (μm)
	P+cathode	6 (μm)

3. Experimental Result

Fig. 2 shows the measured I-V characteristics of the conventional LEST and those of the LEST with the protection circuit. The threshold voltage of the M_P is 2.5 V. The breakdown voltage of the conventional LEST is about 17 V while that of the LEST with the protection circuit exceeds 200 V due to the protection circuit. The forward

voltage drop at 100 A/cm^2 of the LEST with the protection circuit is identical to that of the conventional LEST.

The maximum controllable current (MCC) of the conventional LEST was measured by turning-off the gate voltage from 15 V to 0 V. The measured MCC was 280 A/cm^2. Fig. 2 shows that the maximum current (I_{MAX} in Fig. 2) of the LEST with the protection circuit is under MCC because of the protection circuit, while that of the conventional LEST exceeds the MCC. Even though the proposed protection circuit can not increase the MCC of LEST, the protection circuit can allow the LEST to operate below MCC by adjusting I_{MAX}.

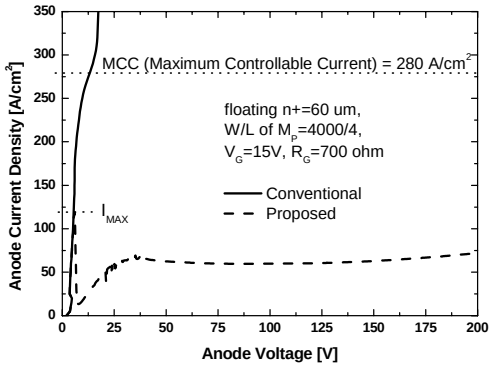

Fig. 2 Experimental I-V characteristics of the conventional LEST and the LEST with the protection circuit

The inner gate voltage (D_P) and the floating n+ voltage (G_P) before and after the activation of the protection circuit measured simultaneously with I-V curve tracing as shown in Fig. 3. Following the anode voltage, the floating n+ voltage increases with time before the activation of the protection circuit. When the floating n+ voltage reaches 2.1 V, which is the threshold voltage of M_P, the inner gate voltage starts to decrease gently. The inner gate voltage is reduced from 15 V to 9 V abruptly when the floating n+ voltage is about 2.5 V. After the activation of the protection circuit as shown in Fig. 3, the floating n+ voltage did not follow the anode voltage further and saturated to around 5.3 V, which was less than the breakdown voltage of the lateral MOSFET. Therefore, the high voltage current saturation exceeded the breakdown voltage of the lateral MOSFET.

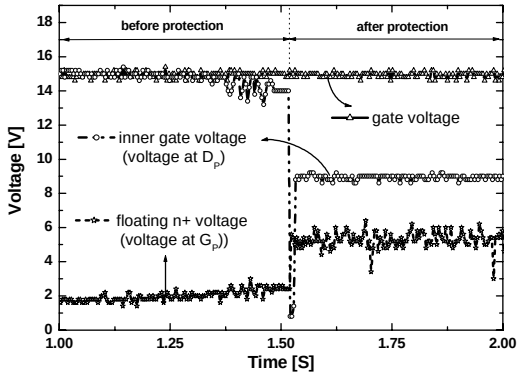

Fig. 3 The inner gate voltage (D_P) and the floating n+ voltage (G_P) before and after the activation of the protection circuit (R_G is 300 Ω and W/L of M_P is 4000/3)

In order to investigate the protection during the practical short-circuit condition, HSF test is performed as shown in Fig. 4. Anode current of the LEST with protection circuit decreases under the MCC, which allows the LEST to withstand over 10 μs during short-circuit while that of LEST without protection circuit increases over the MCC, which induces the junction failure due to the high power dissipation.

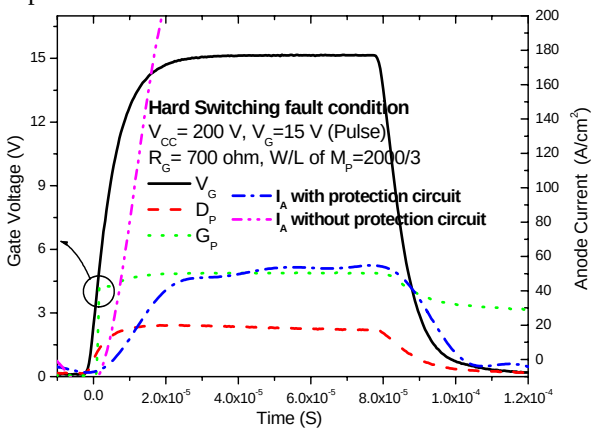

Fig. 4 Waveforms under HSF test

4. Conclusion

A new protection circuit for high voltage current saturation of a lateral emitter switched thyristor (LEST) was proposed and successfully fabricated. By sensing the floating n+ voltage, the protection circuit alters the operation mode of the thyristor from regenerative to non-regenerative. Because the floating n+ voltage does not follow the increasing anode voltage during the non-regenerative operation mode, high voltage current saturation was obtained. Experimental results showed that high voltage current saturation by the proposed protection circuit exceeded 200 V, which was well above the breakdown voltage (~17 V) of the lateral MOSFET in the LEST and also allows the LEST to withstand over 10 μs during the hard switching fault (HSF) condition. Even though the proposed protection circuit could not increase the maximum controllable current (MCC) of LEST, the protection circuit did allow the maximum current of the LEST to be under the MCC.

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