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Wafer-level Fabrication of Compliant Bump

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1. Introduction

Three-dimensional (3D) chip-stacking technology is attracting a great deal of attention for realizing advanced high-speed, compact, and highly functional electronic systems [1–4]. In order to realize the 3D stacked-chip system, a bonding technology that can form a number of bump inter-chip connections is required.

Chip stack bonding using compliant bump[5] has great potential for facilitating 3D chip-stacking because it has the following advantages (Fig. 1); (1) minimizing of pressing load, (2) compensation effect on the bump height deviation and nonuniformity in bonding pressure, which will suppress the bonding failure and reduce the residual strain because the sharp structure of the compliant bump will induce plastic deformation of the bump material, (3) resin exclusion effect in chip-stack bonding of chips with pre-coated resin.

We have fabricated the pyramid bump[5] as one of the compliant bumps using the bump transfer method (Fig. 2). Using the pyramid bump, we confirmed the above mentioned advantages of compliant bump. However, the transfer of bumps is applied to chip-level process. Besides, the perfect bump transfer became difficult when the number of bumps in a chip increased (≥ 10000). Therefore, a new process which can fabricate a number of compliant bumps directly on a wafer is required.

In this paper, we propose the wafer-level fabrication process of compliant bump. A "under-cut resist method" is developed to realize the wafer-level fabrication process. We demonstrate the effect of the new compliant bump on high-density chip-stack interconnection.

2. Wafer-level fabrication of compliant bump

Figure 3 shows the process flow of the "under-cut resist method". First, Ti, W and Au were subsequently deposited as the seed layer for electroplating (Fig. 3(a)). Next, the resist pattern having an under-cut hole profile was formed by photolithography (Fig. 3(b)). The resist used was ZPN1100 manufactured by ZEON corporation. The under-cut profile was controlled by bake temperature and development time. Au electroplating was applied to fill the under-cut holes in the resist film. The photoresist and the seed layer were subsequently removed by a solvent and Ar^+ ion etching, respectively(Fig. 3(c)).

Figure 4 shows the optical micrograph and SEM image of new compliant bumps on a wafer. The number of bumps is 10000 per 2.0×2.0 mm^2 chip. We can see that uniform compliant bumps are formed over the chip area. The bump size is 11 μm in diameter at the basement and the bump height is 10 μm.

3. Effect of new compliant bump

Next, we investigated the new compliant bump in terms of the compensation effect on the bump height deviation and nonuniformity in bonding pressure. In order to investigate the compensation effect on the bump height deviation and the nonuniformity in bonding pressure, we measured the deformation of the bumps after pressing the chip with bumps against a quartz substrate. The pressing condition was as follows: pressing load, 0 $\sim$ 10 kgf (0 $\sim$ 1 gf / 1 bump); temperature at the substrate and chip side, 30°C; pressing time, 20 sec; number of bumps, 10000; chip size, 2.5×2.5 mm^2.

Figure 5 shows the change in bump height with the pressing load for the conventional plated bump, the pyramid bump and the newly developed compliant bump. We found that the change in bump height of the new compliant bump and the pyramid bump are much larger than that of the plated bump. This result demonstrates that the new compliant bump as well as the pyramid bump has a significant advantage over the plated bump in compensating the bump height deviation and the nonuniform bonding pressure.

4. Chip-stack interconnection test

We have tested the new compliant bump for high density chip-stack interconnection. The evaluation was carried out by electrical connection test of daisy chain of bump connections whose number was 2500.

Figure 6 shows the current-voltage characteristic of the plated bump and the compliant bump after bonding of chips with pre-coated resin. The chip bonding condition was as follows: pressing load, 1.25 kgf (0.5 gf / 1 bump); temperature at the chip side, 250°C; temperature at the substrate side, 100°C; bonding time, 20 sec; chip size, 2.5×2.5 mm^2. In the case of the plated bump, daisy chain was open, which can be attributed to the residual resin. On the other hand, in the case of the new compliant bump, daisy chain was successfully connected. This result demonstrates that the new compliant bump offers high-density chip-stack interconnection. The resistance for a bump connection is estimated to be about 7Ω / bump, which is high for applications and, therefore, requires further investigation on bonding condition.

5. Conclusion

As the wafer-level fabrication process of the compliant bump, "under-cut resist method" was demonstrated. It was found that the new compliant bump as well as the pyramid bump has a significant advantage over the plated bump in compensating the bump height deviation and the nonuniform bonding pressure. The newly developed compliant bump process has the potential application to 3D chip-stacking with high-density inter-chip connection.

Acknowledgment

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References

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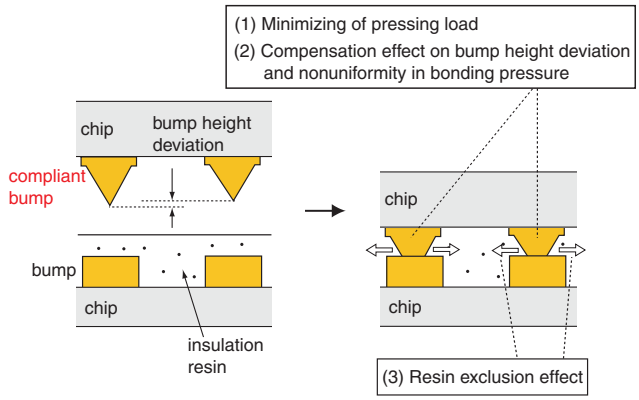

Fig. 1: Advantages of compliant bump.

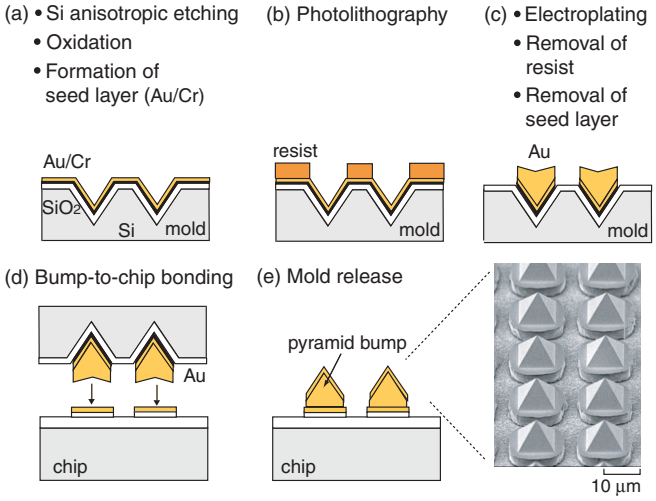

Fig. 2: Process flow of pyramid bump using bump transfer method.

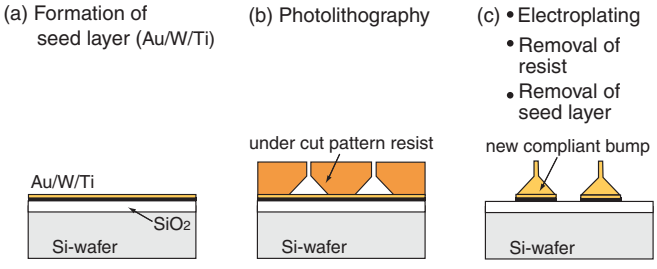

Fig. 3: Process flow of new compliant bump using under-cut resist method. The under-cut pattern profile was controlled by bake temperature and development time. The bump material was Au.

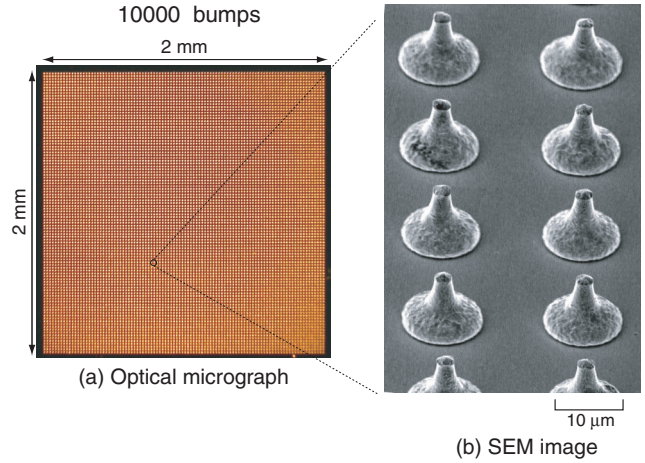

Fig. 4: Optical micrograph and SEM image of new compliant bumps on a chip in a wafer. The bump size is 11 μm in diameter at the basement and the bump height is 10 μm. The number of bump is 10000.

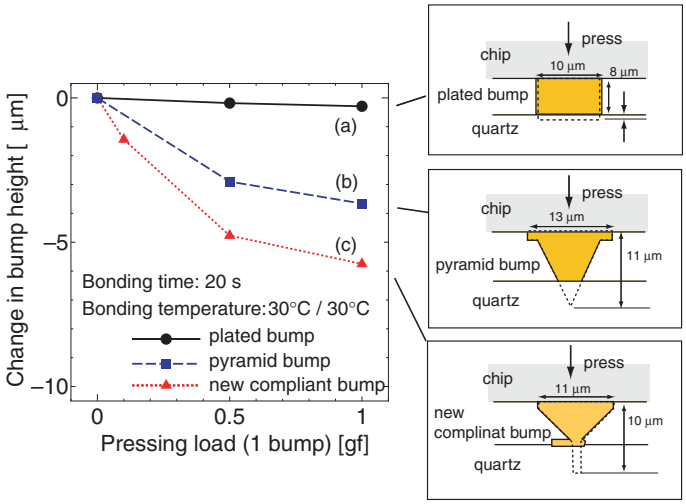

Fig. 5: Change in bump height with pressing load: (a) plated bump. (b) pyramid bump. (c) new compliant bump.

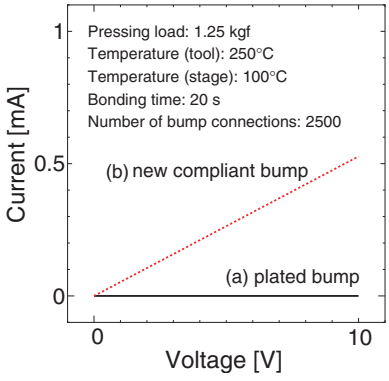

Fig. 6: Current-voltage characteristic of 2500 bump connections of daisy chain after bonding of chips with pre-coated resin: (a) plated bump. (b) new compliant bump. The daisy was open in the case of the plated bump while it was successfully connected in the case of the new compliant bump.