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Integration of 0.45-mm^2 On-Chip-Antenna (OCA) with High Output Power for 2.45GHz RFID Tag

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1. Introduction

For last several years, RFID has attracted widespread attention since it finds more applications beyond being merely a tagging device [1-4]. Nevertheless, several concerns among the end-users exist regardless of the application specifics, namely the cost, size, and performance over distance/area, etc.

The cost of RFID Tag (Transponder) is the major part of RFID system cost in many applications, which could be reduced if the associated antenna can be directly integrated on RFIC chip since the assembling process is not necessary. In addition, it enhances robustness at system level. Due to its battery-less operating mode, sufficient power transmission is required for on-chip-antenna (OCA) on a passive tag-chip. This performance requirement imposes a severe challenge in achieving such since the size of OCA is defined by the underlying small tag-chip area.

Meanwhile, to further reduce the cost of tag-chip, smaller die size is also highly desirable with the anticipation of higher die density and die yield. With the continuing availability of higher density IC (and thus smaller tag-chip area) from the advanced CMOS technology, the fact of OCA size being non-scalable demands an innovative design and fabrication technique to achieve a high-quality antenna.

Abrial et al. reported OCA fabricated on a contactless smart card chip with area 4×4-mm^2 fabricated with 0.25μm CMOS technology [1]. The maximum recovered power was around 18mW from 1W output of the reader, which was sufficient to drive the chip to respond to the reading and writing of the card system working at 13.56 MHz. Another RFID tag with OCA was reported by Hitachi Maxell [2], with working frequency of 13.56 MHz, the operation distance ≤3 mm and the chip area of 2.3×2.3mm^2 fabricated by 0.8-μm CMOS technology. Usami reported on Hitachi's μ-chip, with 2.45 GHz working frequency using gold plating OCA [3]. Unfortunately, there was no detail on OCA related parameters, specifically on its fabrication and device performance. Due to the increasing interest of RFID, some discussion of fabrication technique, challenge, and device performance is required.

In this paper, we present our recent results of OCA for RFID tag working at 2.45 GHz from the process integration and device performance view points.

2. Process Development

Fig.1 shows the cross-section of OCA on a tag-chip. After the tag-chip fabrication, a re-distribution layer (Al) was deposited and patterned, which serves both as re-locating the contact position for OCA and as shielding the interference from the underlying circuits. The antenna was fabricated on a thick undoped-silicon-glass (USG), 15 μm, and connected with the underlying circuits through vias etched in USG. The use of thick USG poses process challenges.

First challenge is how to achieve such thick USG without severe wafer warpage since the warp makes the post processing impossible. The USG was deposited by a conventional PECVD. The ratio of precursors were optimized to achieve the wafer flatness as good as the fresh starting Si substrate. Fig.2 describes the films warpage behaviors over an 8"-Si for 20μm USG before and after the optimization.

Second challenge is the deep via etch through the ultra thick USG connecting the underlying chip and top OCA. The problem is that a trade-off exists between requirements of maintaining selectivity to a mask and avoiding formation of excessive polymer on the bottom of vias resulting in etch-stop. We have developed a special etching scheme with multiple steps by dynamically adjusting oxide/mask selectivity (from high to lower in the etching). Cu/USG single damascene technology has been employed in the fabrication. Fig 3 and Fig. 4 describe the dimensions of via at the top and bottom and the cross section of completed via, respectively.

The OCA was optimally designed and fabricated over a given area of the tag-chip **~1×0.5 mm^2**, which was pre-fabricated in a major foundry with its 0.13-μm CMOS technology. The coil of OCA was fabricated with Cu/USG single damascene technology. **The coil thickness/width is 3/10 μm, with total overlying area of 0.45 mm^2.** The top-view of OCA on a RFID tag is shown in Fig. 5.

3. OCA Performance

The impedance of OCA vs. frequency is shown in Fig. 6, which should be matched with the connected circuit. Because of the shielding layer, the impedance value tested on dummy wafers is consistent with that on virtual wafers. Fig. 7 shows the schematic circuit and top view of rectifier with OCA for V_{DD} test. Fig. 8 presents the V_{DD} vs. RF CW power at 2.4 GHz. **617 μW** of available DC power has been obtained from the output of rectifier as the OCA is inductively coupled with a coil that is driven by a 1W 2.45 GHz CW power source. **To the best knowledge of authors, this is the smallest RFID tag with OCA providing the highest available power reported to date.**

4. Conclusions

OCA has been developed for 2.45 GHz RFID tags with chip area of 0.5 mm^2. The rectified DC power from the OCA and rectifier is sufficient to power the chip.

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References

[1] A. Abrial, J. Bouvier, M. Renaudin, P. Senn and P. Vivet, IEEE J. of Solid-State Circuits, vol. 36, No. 7, 2001, pp.1101-1107.

[2] http://www.hht-igi.com/products/industrial/RFID_CoilOnChip/, 5/4/2005.

[3] M. Usami, Radio Frequency Integrated Circuits (RFIC) Symposium, 2004, Digest of papers, pp.241-244.

[4] http://www.fecinc.com.my/downloads/FEC_MMChip. Press Release, 2nd March 2004.

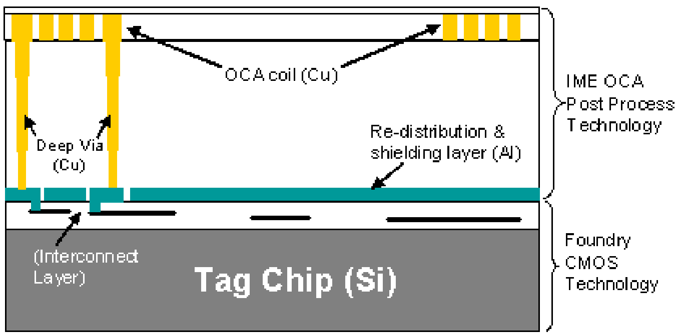

Fig. 1 The cross-section structure of OCA integrated on RFID tag chip.

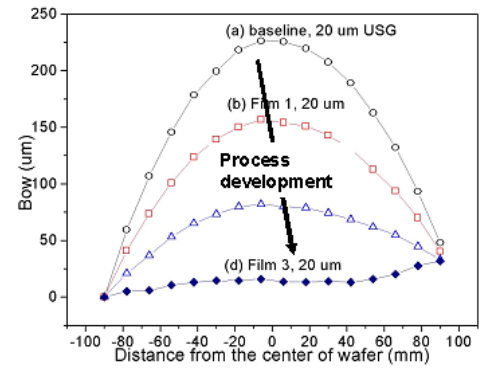

Fig. 2 Wafer warp caused by thick USG deposition before and after process development.

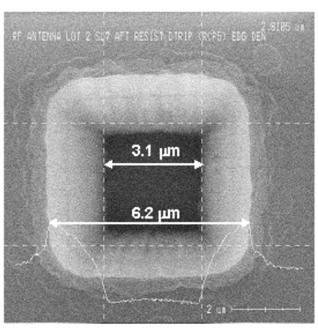

Fig. 3 Top-view of the etched deep via (15 µm) before Cu filling. (CD-SEM picture)

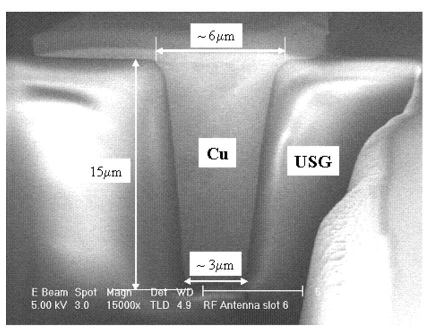

Fig. 4 The cross-section of deep via after Cu filling

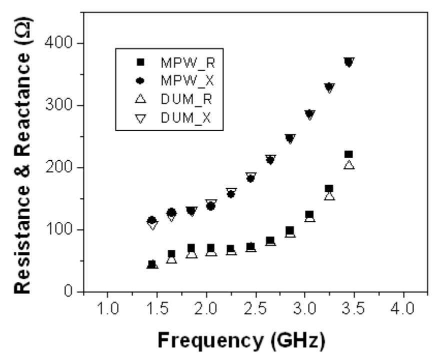

Fig. 6 Impedances (resistance and reactance) vs. frequency; the solid symbols are extracted from the OCA on a real chip wafer, and the hollow symbols on a bare silicon wafer with the same dielectric structure underneath as the real chip wafer.

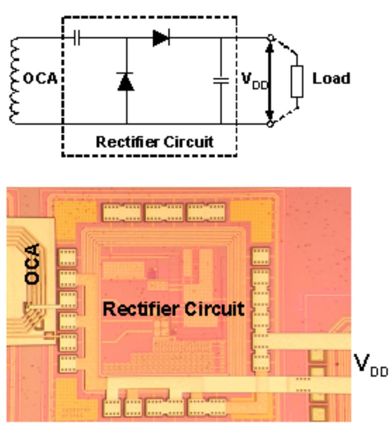

Fig. 7 The schematic circuit and virtual topology of rectifier with OCA for VDD test

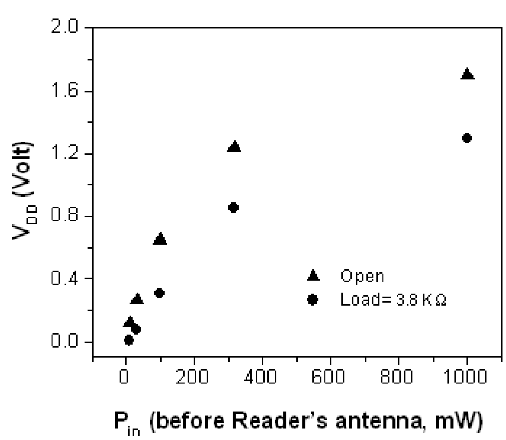

Fig. 8 The output voltage (V_{DD}) extracted from the output of the rectifier.

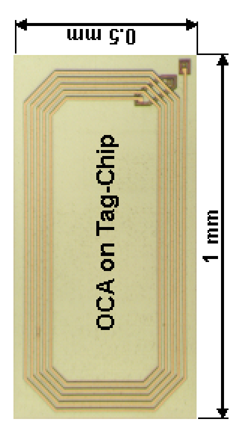

Fig. 5 The top-view of virtual RFID tag with OCA