Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.924-925

D-7-1 (Invited)

Issues of Mixed-Signal Circuit Design in 90nm CMOS LSI Technology

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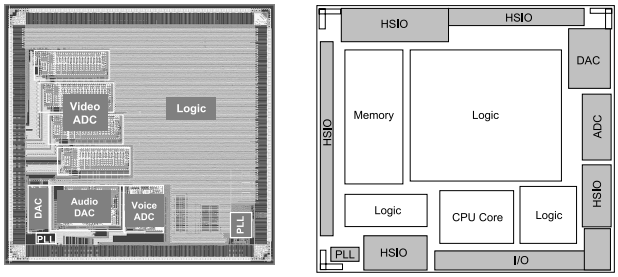
1. Introduction

Whereas digital parts of a SoC become smaller every year with device shrink, the shrink doesn't go ahead in the analog parts because of limitation of operation voltage, therefore the area ratio of analog parts in a SoC becomes bigger year by year (Fig. 1 (a)). Also, high-speed signal processing is accelerated with device shrink of digital parts and it becomes indispensable to integrate a high speed serial interface on a SoC (Fig. 1 (b)). Furthermore, because higher data rate reading is speeded up in a read channel of HD / DVD, power lowing of high speed A/D converter is necessary. Therefore, even in an analog circuit, downsizing, high speed and low power are strongly required in recent years. On the other hand, there are many issues to consider for device shrink and low voltage operation of an analog circuit and the issues will be discussed in this paper taking 90nm CMOS as an example.



(a) (b)

Fig. 1. Examples of SoCs

2. CMOS Technology Roadmap

Road map of CMOS Technology is shown in Fig. 2. Whereas gate density of a SoC rises at about twice of ratio every device generation, power consumption of a digital circuit decreases at a ratio of about 1/2 by lowering supply voltage. Moreover, digital processing speed is increased by about 20–30% every generation. Therefore, device shrink is very attractive for a digital circuit. Fundamentally, device shrink should be attractive for an analog circuit, too. However, the other various factors should be considered for downsizing of an analog circuit.

3. Device Characteristics to be Considered for an Analog Circuit Design

The first problem for an analog design is transistor matching. The gate area dependence of transistor matching is shown in Fig. 3. As transistor oxide thickness becomes thinner with the shrink of transistor, it can be seen that the standard deviation of transistor matching at the same gate area becomes smaller. In other words, gate area can be smaller with thinner oxide transistor, keeping the same matching characteristic. Considering only transistor matching, it is possible to say that device shrink is favorable to an analog circuit design. Next, 1/f noise will be discussed. The relation between transistor input equivalent noise and CMOS technology is shown in Fig. 4. Comparing at the same gate area, it finds that the noise decreases in both NMOS and PMOS with the progress of device shrink. Therefore, thinner oxide transistor is advantageous and device shrink is favorable from the view point of analog area size, if considering only 1/f noise. Comparing with the same capacitance, it seems that 1/f noise is independent of CMOS technology. Third issue is gate leakage current. Fig. 5 shows technology dependence of gate leakage current by tunnel effect. Gate leakage current with minimum length transistor in 90nm CMOS is about 1nA/μm and it will be very serious problem in some circuits such as sample & hold circuit, capacitor memory. In 65nm technology, the gate leakage current will become more by ten times [1]. An example for the measure is shown in Fig. 6. In general, I/O parts are composed of thick oxide transistors and inner circuits are composed of thin oxide transistors in a SoC. Because leakage current of capacitor which composes a loop filter of PLL causes clock jitter, the influence of leakage current can be suppressed to the minimum by using thick oxide transistor for the capacitor. The decrease of distance among wiring metal layers based on device shrink is very serious to digital circuits from delay time point of view. By making the best use of the fault in a digital circuit, fringing (MOM) capacitor can be utilized in stead of MIM capacitor. An example is shown in Fig. 7. If the number of metal wiring layers is 3, the capacitance with unit area will be about 0.9 times of MIM capacitor and almost the same value. As for the matching characteristic, the evaluation result of MOM capacitor is nearly equal to MIM capacitor. Therefore MIM capacitor will be replaced to MOM capacitor in almost of analog circuits and process cost can be reduced in 90nm CMOS and beyond.

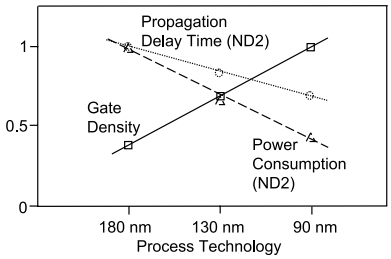


Fig. 2. CMOS technology roadmap

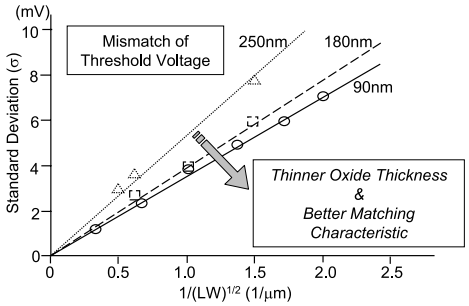


Fig. 3. Matching characteristics (NMOS)

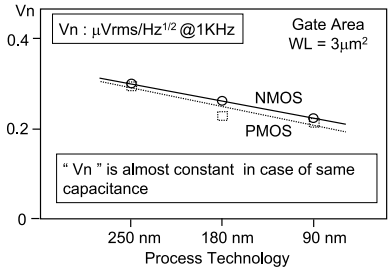


Fig. 4. Input equivalent 1/f noise

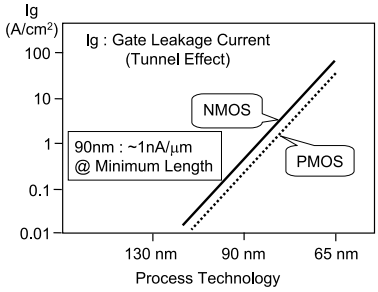


Fig. 5. Gate leakage current

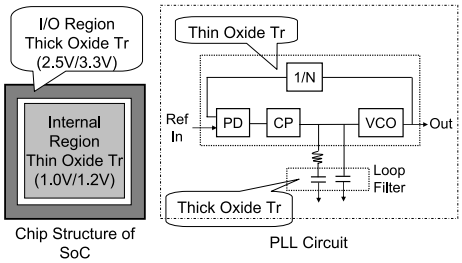


Fig. 6. Measure for gate leakage current

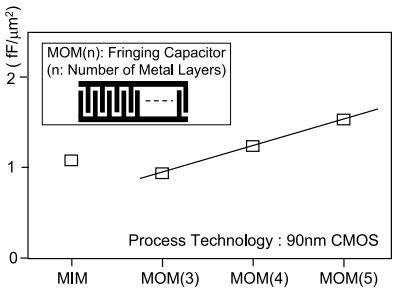


Fig. 7. An example of fringing capacitor

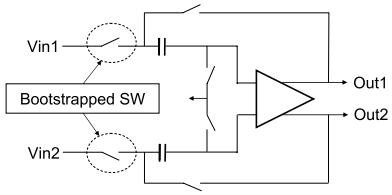


Fig. 8. S/H circuit with Bootstrapped analog switch

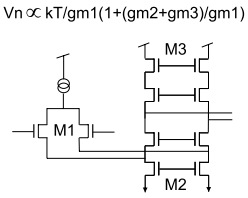


Fig. 9. 1 stage type OP amp

4. Issues on an Analog Circuit Design for Low Voltage Operation

The biggest problem when trying to lower analog operation voltage is an analog switch because of higher impedance at lower voltage. In order to lower the impedance, a bootstrapped analog switch becomes necessary using a thick oxide transistor of I/O parts in a SoC [2]. An example of wide band sample and hold circuit with bootstrapped switches is shown in Fig. 8. Also, when trying to lower operation voltage, the number of transistors in series is limited. The cascade connection of two transistors is generally used for a constant current circuit, but when the cascade connection of two transistors becomes impossible with low voltage, the constant current characteristic degrades. As the result, PSRR (Power Supply Rejection Ratio) becomes lower by the influence of noise from power lines or SoC substrate and clock jitter will become bigger in case of PLL. Therefore, low threshold voltage transistors (Vth = 0.2–0.3V) should be introduced in order to maintain high PSRR at low voltage operation. When trying to lower operation voltage without the change of circuit architecture, consideration of thermal noise becomes necessary [2]. An example of OP amp is shown in Fig. 9. When trying to lower operation voltage, bias current of M1 should not be changed to maintain gain-band width of OP amp. Therefore, channel widths of M2 and M3 should be expanded because gate-source voltage of those transistors becomes lower. As the result, g_m of M2 and M3 become higher and thermal noise of OP amp will increase.

5. Summary

Issues of device shrink in analog circuit design have been discussed taking 90nm CMOS as an example. If excluding gate leakage current, each characteristic of thin oxide transistor is favorable for analog circuit design and improvement of some performances will be expected. The big problem which obstructs device shrink in an analog circuit design is low voltage operation and reconsideration of circuit architecture will become necessary, especially, from the view point of noise.

References

[1] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, pp. 1366–1373, July 2001.

[2] H. Ishii, K. Tanabe, and T. Iida, "A 1.0V 40mW 10b 100MS/s pipeline ADC in 90nm," in *Proc. Custom Integrated Circuits Conf.*, to be published on Sep. 2005.