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A 6-bit A/D Converter for MEMS-control circuit

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1. Introduction

Stacking MEMS structures on a CMOS LSI (CMOS-MEMS) is expected to lead to improved functionality [1-4]. CMOS-MEMS can provide small low-cost devices. We have reported the optical MEMS micromirror switches for a single chip [1]. Fig. 1 shows the proposed structure of our optical MEMS switches, which consists of movable elements (micromirrors), control electrodes, and a MEMS-control circuit. The control circuit operates the movable elements by applying voltages to the control electrodes. But the movable elements vibrate when the control voltage is rapidly changed and it takes a long time for them to stabilize. Moreover, the control voltage for each MEMS device varies, which is related to the fabrication process. To change the position of a movable element to another position quickly without vibration, the MEMS-control circuit needs a feedback-loop technique using a high-speed A/D converter. On the other hand, MEMS devices are operated at over 20 V and the circuit should be developed using a legacy process with high voltage, such as 0.6-μm CMOS technology. Thus, we developed a high-speed A/D converter for the MEMS-control circuit using such a process.

This paper presents a novel circuit technique for the high-speed conversion, which we call the load-veiling circuit technique. We first describe the architectures of the MEMS-control circuit and the A/D converter. Next, the load-veiling circuit scheme is presented. Finally, the experimental results are discussed.

2. A/D Converter in MEMS-Control Circuit

The MEMS-control circuit for optical MEMS switches consists of five blocks as shown in Fig. 1 – position sensors, an A/D converter, a controller, D/A converters, and actuators. The A/D converter and the controller handle all signals of movable elements for low power and compactness. So a high sampling frequency and low delay should be achieved. To operate 100-ch optical MEMS micromirror switches, a sampling frequency of 200 MHz or higher is needed.

With a legacy LSI process, it is easy to construct an A/D converter using sample/hold and positive-feedback circuits (Fig. 2) [5]. In this figure, it is a single-end converter but a differential one is also easy to construct. The converter uses non-overlapped two-phase clocks, $\phi1$ and $\phi2$. The comparator has two periods, sampling and comparison. In the sampling period, the switches operated by clock $\phi1$ are on and the comparator stores charges in the sample/hold capacitors according to the input voltages. In the comparison period, the switches operated by clock $\phi2$ are on and the positive-feedback circuit compares the voltages. However, A/D conversion using conventional comparators is slow because the sample/hold capacitors behave as loads for positive-feedback circuit. Thus, we propose a new technique that suppresses the capacitance influence by introducing a switch function.

3. Fast Comparator with load-veiling switches

Fig. 3 shows a schematic of the proposed comparator. It is a fully differential comparator and consists of sample/hold circuits (block A) and a positive-feedback circuit (block B). In order to veil the sample/hold capacitors for high conversion speed, two switches, S1 and S2, are connected to node X. When the timing comparison period starts, node X is powered and the circuit begins to compare. After a while, S1 and S2 are turned off by the voltage of node X and the connection between the sample/hold capacitors and the positive-feedback circuit is cut off. This accelerates the comparison speed. Fig. 4 shows simulated comparison speeds of the conventional comparator and the proposed one. In the simulation, two input voltages, Vin+ =1.701 V and Vref+ = 1.702 V, were input. The comparators are the same size. The results indicate that the proposed one finishes comparison about three times faster than the conventional one.

4. Experimental Results

We developed the A/D converter using a 0.6-μm CMOS process. Fig. 5 shows a microphotograph of the chip. The core size is 2.6 x 2.1 mm^2, which can be integrated in a single chip with optical MEMS switches. Table 1 shows the specifications of the chip. The maximum sampling frequency is 230 MHz, which is high enough to reduce the settling time of movable elements. Fig. 6 shows a spectrum of the output of the converter with an input signal of 2 MHz at a sampling frequency of 100 MHz. The signal to noise and distortion ratio (SNDR) is 30.5 dB. The power consumption is 271 mW at the maximum sampling frequency of 230 MHz. The experimental results reveal that the load-veiling switches are effective with comparator.

5. Conclusions

A novel high-speed A/D converter for MEMS-control circuit has been developed. We proposed a load-veiling technique for comparator. The developed A/D converter has a SNDR of 30.5 dB and a maximum sampling frequency of 230 MHz using a 0.6-μm CMOS technology.

In conclusion, the A/D converter is suitable for CMOS-MEMS devices.

Acknowledgments

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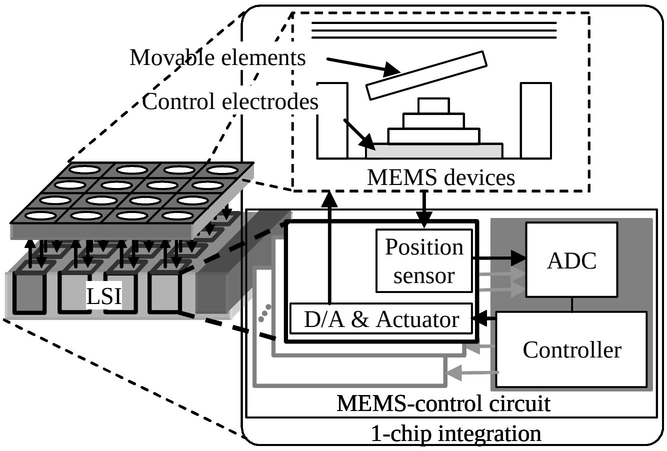

Fig. 1. Proposed structure of optical MEMS switches.

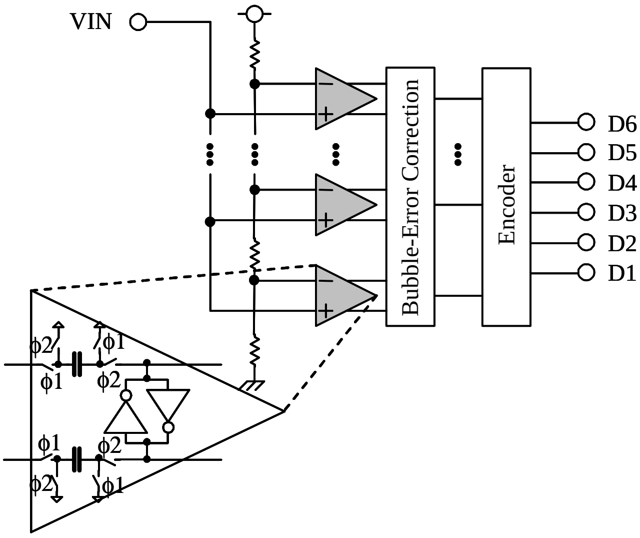

Fig. 2. Block diagram of A/D converter with conventional comparators.

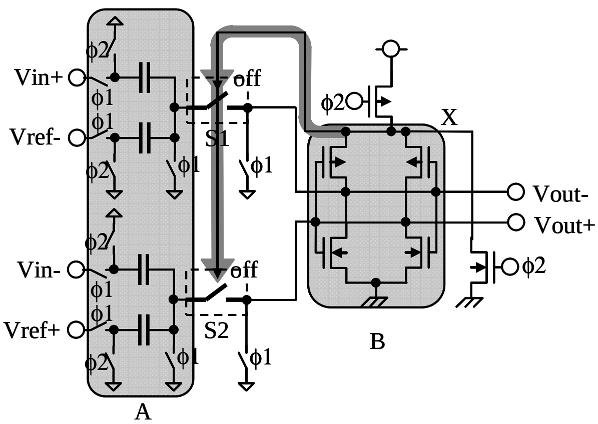

Fig. 3. Proposed comparator with load-veiling switches and its operation.

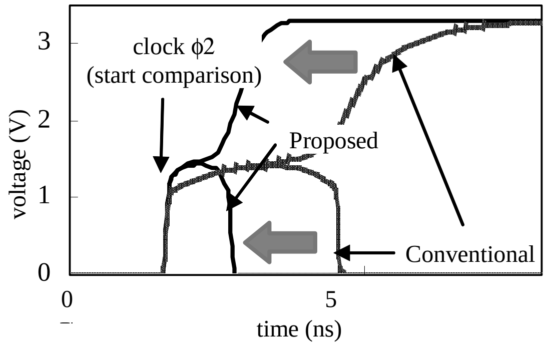

Fig. 4. Comparison between a conventional comparator and the proposed one (Vin+ =1.701V, Vref+ = 1.702V).

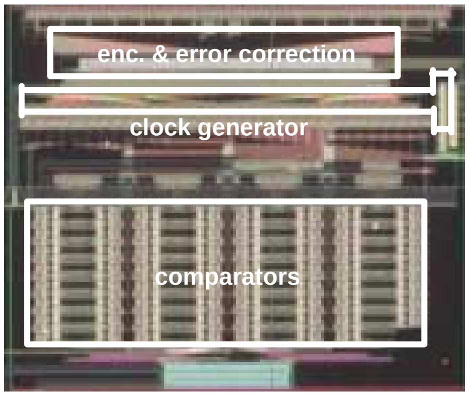

Fig. 5 ADC chip microphotograph.

Table 1. Specifications of the ADC.

Process	0.6 µm CMOS
Resolution	6 bits
Sampling Rate	Up to 230 MHz
Supply Voltage	3.3 V
Power	271 mW @ 230 Msps
Active Area	2.6 mm x 2.1 mm

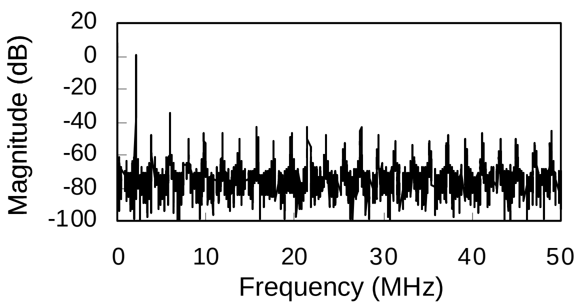

Fig. 6 Spectrum of the ADC output (Fin = 2 MHz, Fsamp. = 100 MHz).