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Low Power and High Sensitivity MRAM Sensing Scheme with Body Biased Preamplifier

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1. Introduction

In recent days, rapid development of mobile and multimedia applications are accelerating the demand for a unified memory technology. Magnetoresistive random access memory (MRAM) is one of the emerging nonvolatile memories with features such as fast read and write access time, high density, and high endurance [1].

To realize these features, low power and high sensitivity MRAM sensing scheme is highly required. Because, MRAM with ultra low power voltage is demanded to beyond the limitation of static random access memory (SRAM) characteristics, and also, the output difference of MRAM between data "0" and data "1" is very lower than that of SRAM and Flash memory. Especially, the MR (MagnetoResistive) ratio, that is a function of the output difference, of a conventional MRAM is limited to less than only several tens of percents. Therefore, novel sensing scheme and sensing circuit are needed in addition to conventional CMOS voltage sense amplifier.

Several sense amplifiers have been proposed and implemented with MRAM[2][3][4], but low voltage operation had not been considered. In this study, we present a new sense amplifier for MRAM with body biased preamplifier, which enables low power and high sensitivity read operation.

2. Configuration of Proposed Body Biased Preamplifier

Figure 1 shows a conventional and proposed MRAM sense amplifier. Conventional sense amplifier.[2], which is shown in Fig. 1(a), consists of two stage of amplifier. First stage is a common-gate stage, which senses the difference of magnetic tunnel junction (MTJ) resistance. The preamplifier also takes on a role of clamping bitlines voltage and MTJ bias. And then, second stage sense amplifier. senses the output of the first stage preamplifier. In this scheme, the main issue is that lack of operation margin with low power operation with low power voltage. On the other hand, current sense amplifier[5][6], which is shown in Fig. 1(b), is widely used to enhance sensing speed.

Figure 1(c) shows the proposed sensing scheme. Proposed sense amplifier consists of body biased preamplifier and second stage sense amplifier. The preamplifier clamps bitlines and MTJ bias appropriately, and also amplifies difference of MTJ resistance utilizing negative feedback current sensing scheme between bitlines and substrate of transistors, which consist of preamplifier, on the same time. Additionally, body effect reduces threshold voltage of the transistors. Therefore, compared to the conventional preamplifier, the proposed circuit enables the reading operation with lower power voltage and higher speed.

3. MRAM MTJ Cell Modeling for Reading

To evaluate the proposed circuit, MTJ resistance characteristics modeling was employed with VHDL-AMS, and proposed circuit was simulated with mixed signal circuit simulator. MTJ I/V characteristics, which is shown in Fig.2, is presented by following Simmons tunneling formula[7](1) with spin direction ϕ.

$$\begin{cases} I(\phi=\pi)=S\theta_s\left(V+\gamma_s V^3\right) \\ I(\phi=0)=\left(1+\dfrac{MR(V)}{100}\right)S\theta_s\left(V+\gamma_s V^3\right) \end{cases} \quad (1)$$

Where, θ_s=2.56×1010, γ_s=0.433, and S stands for the MTJ area. And then, $MR(V)$ is MR ratio dependency on MTJ bias voltage V, which is obtained by following polynomial approximation (2).

$$MR(V)=C_1V^3+C_2V^2+C_3V+C_4 \quad (2)$$

Constants C_1, C_2, C_3 and C_4 in (3) are invoked from experimental results [8][9]. This $MR(V)$ approximation result is shown in Fig.3. From these MTJ resistance models, which are dependent on bias voltage, MRAM cell and sense amplifier can be simulated with high accuracy.

4. Simulation Results and Discussions

Figure 4 shows a circuit diagram for the MRAM reading simulation with proposed body biased preamplifier. On Fig. 4, M9 and M10 are preamplifier circuit. The voltage of the MTJ bias is clamped less than 300mV by adjusting V_{ref}. Second stage CMOS sense amplifier consists of M3-M8. For the conventional sense amplifier, body of M9 and M10 were connected to 0V. Figure 5 and 6 shows the simulation result. Figure 5 shows simulation waveforms at 1.8V power voltage and Fig. 6 shows simulated reading access time against the power voltage. Simulation parameters are shown in Table 1. From Fig. 6, it is shown that proposed sense amplifier is 1.57 times faster than conventional one at 1.35V power supply and also power voltage of proposed circuit is lower for same access time.

5. Conclusions

A novel low power and high sensitivity MRAM sensing scheme with body biased preamplifier was proposed and successfully simulated with 0.18μm CMOS technology. The proposed sensing scheme presented 1.57 times faster access time than conventional scheme at 1.35V power voltage and power of the sense amplifier was lower than conventional one at same speed.

Acknowledgement

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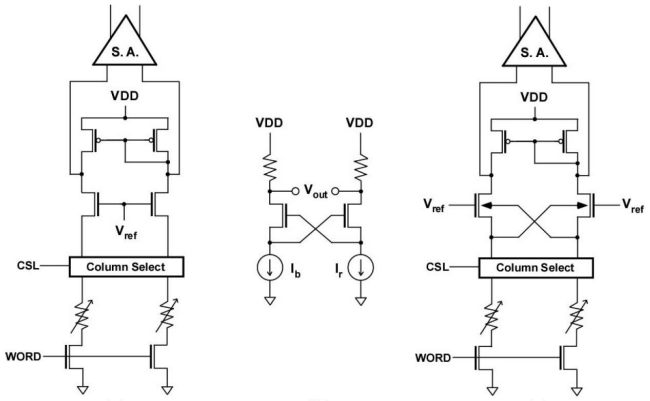

Fig. 1. Configuration of MRAM sense amplifier.

(a) Conventional sense amplifier.

(b) Current sense amplifier reported in [5] and [6]

(c) Proposed sensing scheme with body biased pre- amplifier

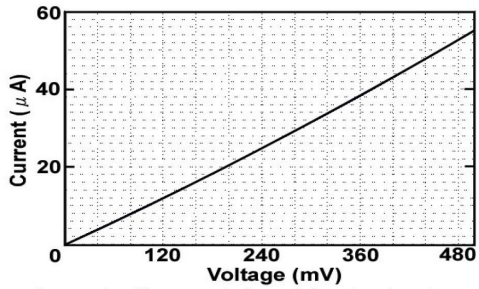

Fig. 2. I/V Characteristics of the simulated MTJ ($1/S\ \theta_s$=5kΩ, γ_s=0.433)

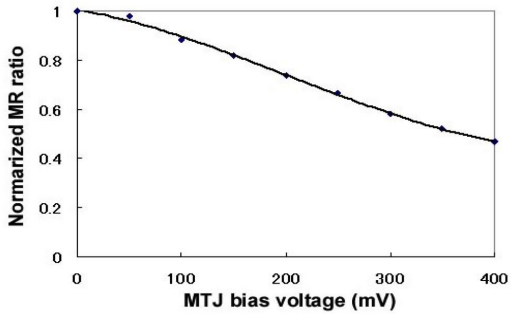

Fig. 3. Approximated simulation model of the dependence of MR ratio on the MTJ bias voltage

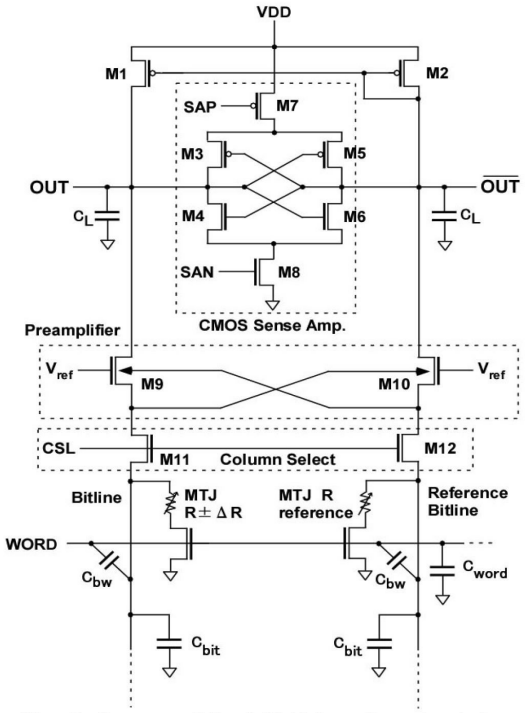

Fig. 4. Circuit diagram of the MRAM reading simulation circuit with proposed body biased preamplifier

Table 1. MRAM Reading Simulation parameters

Power Supply	1.35～1.8V
Technology	0.18μm CMOS
MTJ Resistance	10kΩ
MR Ratio	40%@300mV / 68.9%@0V
Sense Amplifier. Load Capacitance	C_L = 50 fF
Bitline Capacitance	C_{bit}=200 fF
Wordline Capacitance	C_{word}=1.2 pF

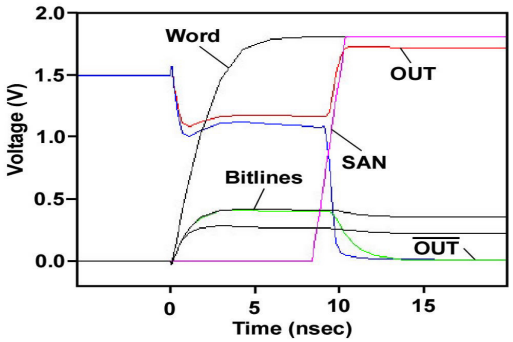

Fig. 5. Simulated waveforms (Vdd=1.8V)

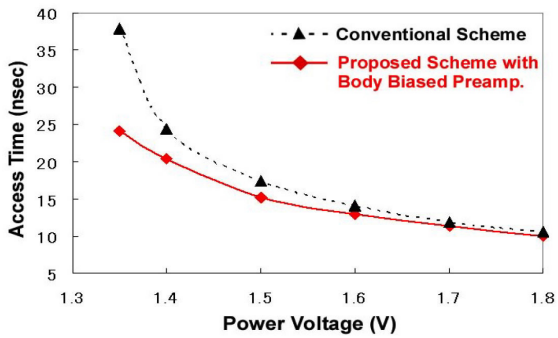

Fig. 6. Simulation result of MRAM reading access time