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A Spurious Suppression Technique for Fractional-N Frequency Synthesizers

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I. Introduction

Low phase noise and fast lock time are required characteristics in PLL frequency synthesizers used in high-speed wireless communication systems. A valid approach for achieving both low phase noise and fast lock time, would be to increase the reference frequency. In conventional integer-N synthesizers, however, the maximum value of the reference frequency is limited by the separation frequency between adjacent channels. In the case of fractional-N synthesizers, reference frequency can be increased without the restriction, but fractional-N synthesizers generate large spurious caused by fractional operation. In this paper, a spurious suppression technique for fractional-N frequency synthesizer is proposed.

II. Circuit design

Fig. 1 shows a block diagram of a typical fractional-N synthesizer, and Fig. 2 illustrates the operation of fractional-N synthesizers. In this case, the division ratio is N+1/4. Because of the fractional operation, the charge pump sends periodic output currents (I_{CP}) whenever PLL is in the locked state. This periodic I_{CP} modulates VCO and causes large spurious.

Fractional spurious suppression techniques have been proposed in [1], [2], where a current compensation circuit is added to the charge pump to suppress the undesired periodic I_{CP}. Fig. 3 (a) shows the charge pump circuit with the current compensation circuit. The compensation current (I_S) is controlled by switching MOS transistor (M1).

Fig. 3 (b) and (c) show simulated results of I_S. When the charge pump output voltage (V_{CP}) is low, desired compensation current is applied to the charge pump shown in Fig. 3 (b). However, when V_{CP} is high, undesired spike appears in the I_S shown in Fig. 3 (c). The drain voltage difference between M1 and M2 cause the change of the drain-source voltage of M3 when M1 and M2 are switched. It induces the current spike and consequently preventing spurious suppression.

To suppress this current spike, we propose the addition of a voltage follower circuit to the current compensation circuit. The voltage follower circuit keeps the drain-source voltage of M3 constant when M1 and M2 are switched.

Fig. 4 (a) shows the proposed circuit diagram and Fig. 4 (b), (c) show the simulated results of I_S. The voltage follower circuit consists of an op-amp and a buffer circuit. The drain voltage of M2 is kept the same value as that of M1. Therefore, undesired current spike can be suppressed in the proposed circuit whenever V_{CP} is high.

III. Measured results

A fractional-N frequency synthesizer using the proposed spurious suppression technique is fabricated using a 0.6-μm SiGe-BiCMOS process. Fig. 5 shows a die photograph of the proposed synthesizer.

Fig. 6 shows the measured output spectrum. The circles indicate the results when the current compensation circuit is inactive, while the line indicates the results when the proposed current compensation circuit is active. Using the proposed circuit, enough spurious suppression is achieved. Fig. 7 shows the measured phase noise, and the integrated phase noise from 10kHz to 10MHz is -32.9dBc.

Table. I summarizes measured results for the proposed synthesizer.

TABLE I
Summary of measured results

Parameter	Value	Unit
Output frequency range	4890 - 5350	MHz
Reference frequency	20	MHz
Channel step	2.5	MHz
Integrated phase noise (from 1kHz to 10MHz)	< -32.9	dBc
Fractional spurious@2.5MHz	< -55.3	dBc
Reference spurious@20MHz	< -57.9	dBc
Lock time	< 100	μsec
Power supply	2.9	V
Current consumption	21	mA

IV. Conclusion

In this paper, a spurious suppression technique for fractional-N frequency synthesizers is proposed. Using the proposed technique, the spurious resulting from the fractional operation can be suppressed sufficiently over a wide V_{CP} range. The measurement results indicate that the proposed technique is useful.

References

[1] D. Banerjee: PLL Performance, Simulation, and Design 3rd Edition (2003)
[2] R. E. Best: Phase-Locked Loop Theory, Design, and Applications, 5th Edition, McGraw-Hill (2003)

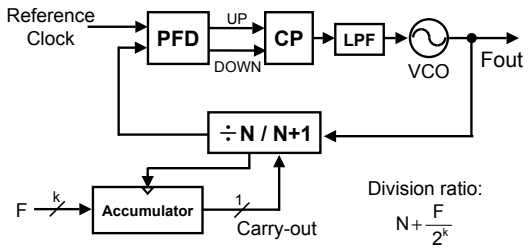

Fig. 1. Block diagram of a typical fractional-N frequency synthesizer

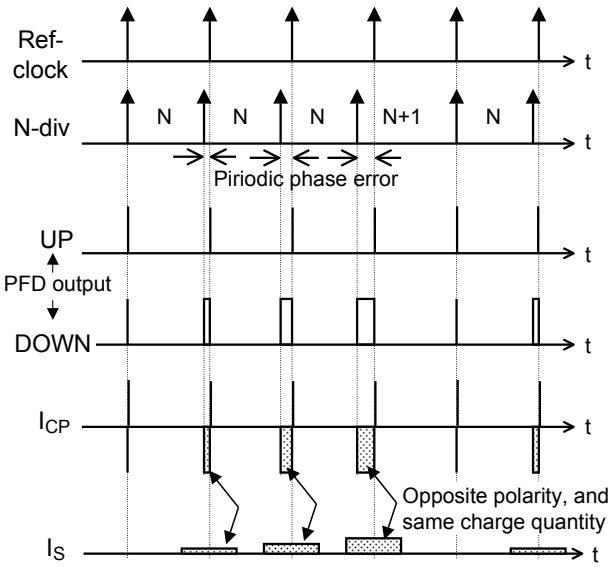

Fig. 2. Operation of a fractional-N synthesizer

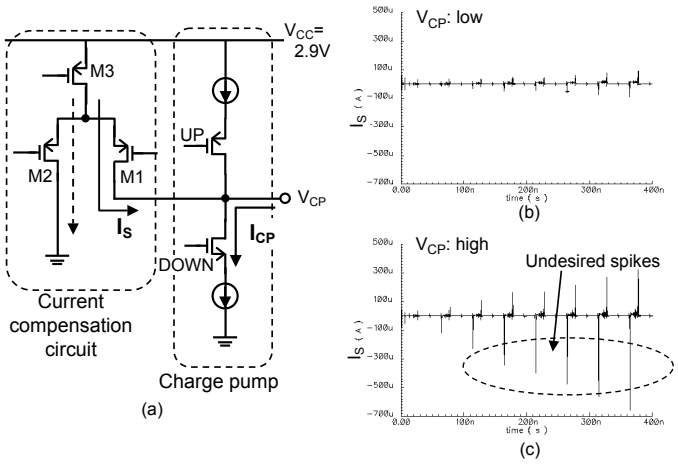

Fig. 3. Conventional current compensation circuit and simulated results of I_S

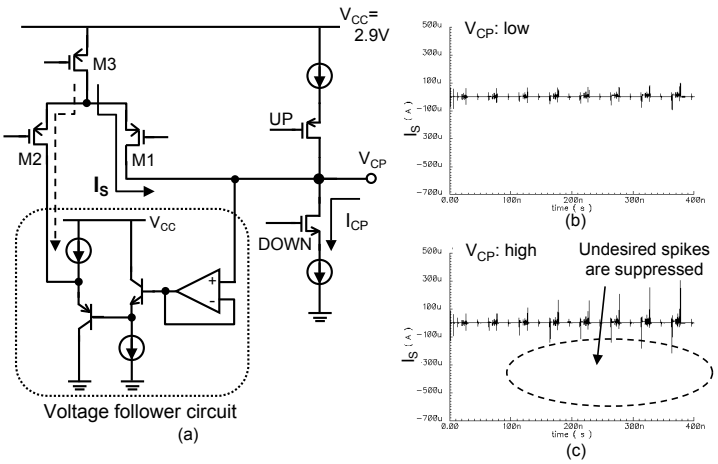

Fig. 4. Proposed current compensation circuit and simulated results of I_S

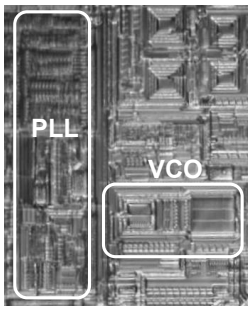

Fig. 5. Die photograph of proposed fractional-N synthesizer

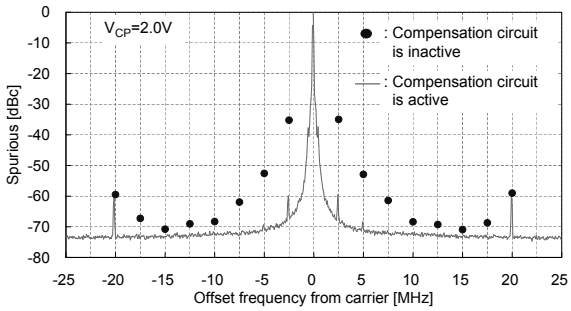

Fig. 6. Measured output spectrum

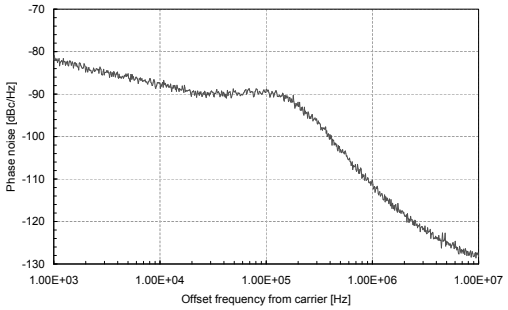

Fig. 7. Measured phase noise