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Design of I-Q down-converter in CMOS for wireless network application

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I. Introduction

One of the critical block in the design of the transceivers is the down conversion mixer. For low-IF architecture, circuit level rejection of image is a challenge. The low-IF quadrature signal processing circuit requires high phase and amplitude accuracy to separate the image signal from the down converted RF signal. A DQM (double quadrature mixer) as proposed and implemented in references [1], achieves a low phase and amplitude imbalance without any external tuning or trimming at 900-MHz. The implementation of DQM in [1] was based on passive mixer. However, at 5-GHz band, RF-LO isolation required is higher, hence, active implementation of DQM is preferred. Active mixer also needs lower RF and LO power than its passive counterpart. Those, single stage of poly-phase generator and lower LO drive can be implemented without sacrificing the total noise figure of the receiver. Using Monte Carlo analysis, [2], performance of the DQM as a function of the phase and amplitude mismatch variation is simulated. Normal distribution is assumed with 10% and 5^o tolerances for amplitude and phase mismatch respectively. These tolerances are typical values for single stage RC polyphase filter. Fig. 1 shows the plot of R and R_d probability distribution of IRR (image rejection ratio). It is interesting to note that with perfect mixing, DQM shifts the IRR distribution to double with more wider probability. In other words, the sensitivity of the IRR due to the mismatch is reduced or averaged out. We thus expect very low mismatch in quadrature signal from the DQM.

II. Circuit Implementation

The block diagram of the DQM implementation is depicted in Fig. 2. The I-Q signals from RF and LO are both generated by RC-CR polyphase filter. The mixing process is carried out by the four identical mixers, and the output I-Q signals are summed to produce I-Q IF signals for baseband processing. Double-balance Gilbert cell is employed at the active mixer. Use of buffers at the input stages of the DQM have been omitted to minimized the device mismatches. However, impedance matching becomes an critical issue as the RF polyphase filter directly couples to the high impedance input port of the DQM. Fig. 3 shows the circuit implementation of the Gilbert cell with inductive degeneration using dual current sources. The on-chip spiral inductor is used in differential mode, [3], hence, higher quality is obtained in comparison with two inductors in single current source Gilbert cell. The area occupied by the differential spiral inductor is also at least half of the two inductors'. This approach is very important in DQM as four mixers are employed. Besides impedance matching, the use of the inductor provides better trade-off between mixer's conversion gain and NF (noise figure) with the linearity, [4]. However, existence of the capacitive parasitic, C_p, (as shown in Fig. 3), limits the inductor value used as far as stability is concern. If the series resistance of the spiral inductor is made negligible, L_s should be less than $2/(\omega^2 \cdot C_p)$, where ω is the operating frequency. As the DQM is highly insensitive to the mismatch in the quadrature signals, a simpler circuit topology was used for the quadrature generation. The RF quadrature signals are generated through a passive RF poly-phase filter constructed in a RC-CR structure. The RF polyphase filter is the first stage of the DQM, hence its insertion loss contribute significantly to the overall noise figure. A single stage polyphase filter is adopted to keep the noise figure to a minimum. The single stage polyphase filter has narrow bandwidth and its phase and amplitude error away from the center frequency can be large. However this phase and amplitude errors are well suppressed by the DQM. The RC-CR structure reflects a real and reactive impedance to the source. The values of RC-CR were chosen to give a real part of impedance of 50Ω to the source. The reactive part of the impedance is match to its conjugate by the circuit transmission line and bond wire. This eliminate the matching circuit and hence reduces the chip area.

III. Measurement Results

The designed DQM was fabricated in a standard digital 0.18-μm CMOS process. Fig. 4 shows the microphotograph of the DQM, with core area of 1.30-mm×2.40-mm. The RF signal interconnects were modeled as transmission line during post-layout simulation in the design phase. For better accuracy, these transmission line characteristics were estimated from the measured data. Hence, only specified dimension of interconnects were employed. The input return loss is more than 12-dB across a pass-band of 5.15 to 5.35-GHz. The amplitude and phase mismatch of the I-Q signal at IF correspondences to the input RF frequency input is depicted in Fig. 5. Fig. 6 shows the measured conversion gain and NF, the DQM has a typical NF of about 18-dB, at conversion gain of 10-dB. The measured performance of the DQM is summarized in Table I.

IV. Conclusion

The design and implementation of the 5-GHz down-converter for low-IF application in standard digital CMOS technology is described. DQM architecture with improved device matching technique is employed to achieve high accuracy of amplitude and phase matching. Measurement results show less than 0.5^o and 2% phase and amplitude mismatch between the output quadrature signals within the desired pass-band.

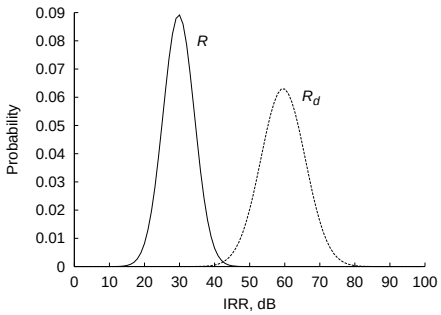

Fig. 1. Probability distribution of IRR

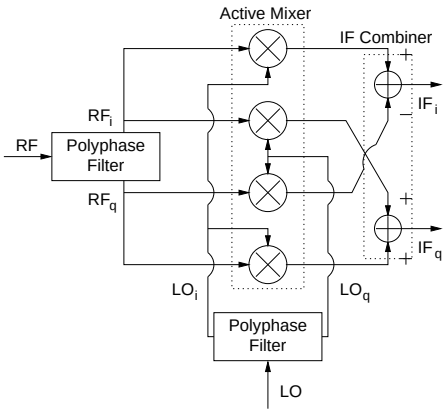

Fig. 2. DQM block diagram, *i*:in-phase signal, *q*: quadrature-phase signal

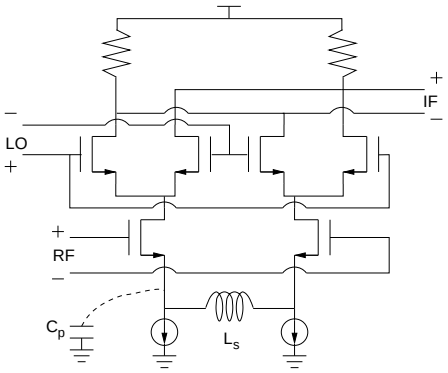

Fig. 3. Active mixer using Gilbert cell

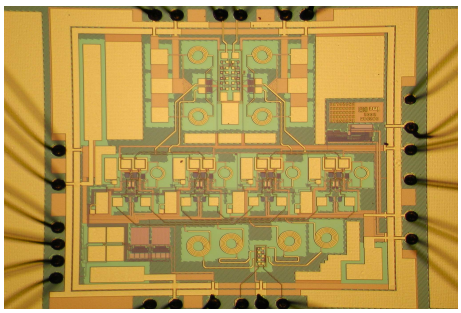

Fig. 4. DQM microphotograph

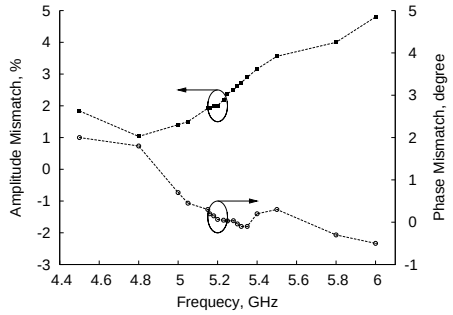

Fig. 5. Measured quadrature signal mismatch, at output of the IF combiner

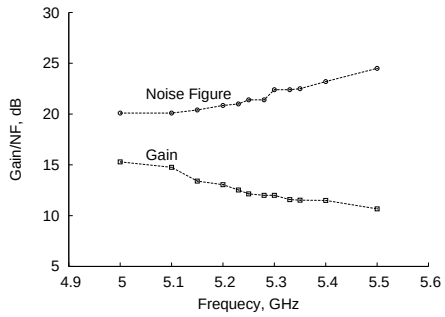

Fig. 6. Measured conversion voltage gain and noise figure, at output of the IF combiner

ACKNOWLEDGEMENT

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TABLE I

MEASURED PERFORMANCE OF THE DQM

Parameter	Measurement Result
Supply Voltage	1.8V
Drain Current	12.0mA
Voltage Conversion Gain	15.0dB
IIP3	-2.5dBm
NF	$<$20dB
Phase Error	$<0.3^o$
Amplitude Mismatch	$<$0.4dB
Input Return Loss (5.15-5.35GHz)	$>$12dB