Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.936-937

D-8-4

Zero-Crosstalk Bus Line Structure for Global Interconnects in Si ULSI

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1. Introduction

The International Technology Roadmap for Semiconductors has predicted that global interconnect delay becomes much larger than gate delay annually [1]. The global interconnects are conventionally designed as an RC line, and more repeaters are required for longer global interconnects [2]. Power consumption and delay time are proportional to a line length. It is a significant issue to reduce delay time and power consumption in global interconnects simultaneously.

This paper proposes a novel technique to achieve high-speed signal transmission, low power consumption and high-density on-chip bus line using differential transmission lines (DTL). Generally, there is a trade-off between a wiring pitch and crosstalk robustness. We show the high-density bus line structure that can achieve zero crosstalk-noises. The feasibility of the proposed structure is discussed using results from a two-dimensional electromagnetic simulator (2D Extractor, Ansoft) and a time-domain measurement.

2. Differential transmission line

We have proposed to use a differential transmission line (DTL) as the global interconnect in Si LSIs [3]. The DTL can achieve both high-speed and low power consumption compared with RC interconnects. In the transmission line (TL), signal can propagate with an electromagnetic-wave speed along TLs. Power consumption does not depend on signal frequency and line length because the DTL interconnect does not require repeaters. DTLs have high common-mode crosstalk robustness, and faster circuit operation can be achieved with DTLs than with single-ended transmission lines (STL). DTLs are suitable rather than STLs from the view point of implementation in the multilevel interconnect structure, because DTLs do not require ground plane [4]. However, DTLs require larger wiring area than RC lines because DTLs use two signal lines per one signal. To reduce wiring area is essential to embed a lot of DTLs in multilevel interconnects. We have already reported around 4 Gbps signal transmission using 2.5 mm-long DTL with $0.35\ \mu\mathrm{m}$ CMOS driver and receiver circuits [5].

3. Proposed Bus Line Structure

Figures 1 and 2 show a schematic and a structure of the proposed bus line. The bus line consists of diagonal-pair and stacked-pair lines, which can transmit 4 signals using 6 lines. Differential pairs (D1 and $\overline{\mathrm{D1}}$), (D2 and $\overline{\mathrm{D2}}$) and (S1 and $\overline{\mathrm{S1}}$) are used for differential-mode transmission. Diagonal-pair lines in the same set, e.g. (D1 and $\overline{\mathrm{D1}}$) and (D2 and $\overline{\mathrm{D2}}$), are not influenced by crosstalk noise, and differential-mode crosstalk noises ideally become zero. The stacked-pair line (S1 and $\overline{\mathrm{S1}}$) shields crosstalk noises from other sets of diagonal-pair lines. The common-mode signal of these lines D1, $\overline{\mathrm{D1}}$, D2, $\overline{\mathrm{D2}}$, S1 and $\overline{\mathrm{S1}}$ can be used for common-mode transmission. The common-mode transmission uses a signal line and reference voltage such as the pseudo differential transmission [6]. The common level of D1, $\overline{\mathrm{D1}}$, D2, and $\overline{\mathrm{D2}}$ can be used as the signal line, and the common level of S1 and $\overline{\mathrm{S1}}$ can be used as the reference voltage as shown in Fig. 2.

Figure 3 shows principle of noise cancellation in the set of diagonal-pair lines. DTLs have positive and negative signal lines. If distances from a victim to positive and negative aggressor lines are the same, crosstalk noises from positive and negative lines counteract each other at the victim because these aggressor lines have mutually reversed phases. Thus, differential-mode and common-mode crosstalk noises become zero at diagonal-pair lines.

4. Characteristics of Proposed Bus Line

In designing TLs, (1) attenuation, (2) layout area and (3) crosstalk robustness are the most important considerations. Parameters of $65\ \mathrm{nm}$ technology node for MPU in the ITRS are used [1]. It is assumed that the number of metal layer is eleven. The metal is copper. An interlayer dielectric has a relative dielectric constant of 2.3. The bus line is implemented in global layers. Thicknesses of metal and dielectric at global layer are assumed to be $0.8\ \mu\mathrm{m}$. Line widths and line-to-line distances of diagonal-pair lines are determined by thicknesses of metal and dielectric considering the principle of noise cancellation as shown in §3. Diagonal-pair lines have widths of $0.8\ \mu\mathrm{m}$ and line-to-line distances of $0.8\ \mu\mathrm{m}$. The stacked-pair line has a width of $0.8\ \mu\mathrm{m}$. Figure 4 shows time-domain measurement results of DTL . The DTL has a line length of $1\ \mathrm{mm}$, a line width of $0.8\ \mu\mathrm{m}$ and differential impedance of $100\ \Omega$. The measurement results exhibits that the DTL can transmit $12\ \mathrm{Gbps}$ signal. It is expected that proposed bus line can transmit over $10\ \mathrm{Gbps}$ signal.

The proposed bus line structure is examined using the two-dimensional electromagnetic simulator. Distances between diagonal-pair lines and stacked-pair lines D_p in Fig. 2 are determined by crosstalk robustness. A crosstalk coefficient is used to estimate crosstalk robustness as shown in Fig. 5. K_f and K_b are forward and backward crosstalk coefficients, respectively. A bit rate is $10\ \mathrm{Gbps}$, a rise time t_r is $20\ \mathrm{psec}$ ($t_r = 0.1/(5\ \mathrm{GHz})$). The line length is assumed to be $1\ \mathrm{cm}$. The crosstalk margin is assumed to be $|\mathrm{crosstalk\ coefficient}| < 0.1$. Figure 5 (b) shows crosstalk coefficients as a function of D_p. Crosstalk coefficients between diagonal-pair lines in the same set, K_bDD and K_fDD, are not zero because of influences of adjacent stacked-pair lines. K_bDD and K_fDD decrease as a distance D_p increases. All of crosstalk coefficients satisfy the crosstalk margin over $0.8\ \mu\mathrm{m}$. Differential impedances of the diagonal-pair and stacked-pair lines are designed to be $100\ \Omega$ and $80\ \Omega$, respectively. Characteristic impedance of PDTL is designed to be $30\ \Omega$.

Figure 6 shows signal attenuation characteristics as a function of signal frequency. The attenuation increases as frequency increases. The attenuation of the stacked-pair line and PDTL are larger than that of the diagonal-pair line because of smaller characteristic impedance. PDTL has almost the same attenuation as the stacked-pair line. PDTL has four times

larger cross-sectional area than the stacked-pair line although the PDTL has smaller characteristic impedance than DTLs.

Figure 7 shows line pitches per one signal. The line pitch of proposed structure is compared to that of a co-planar line that has the same crosstalk robustness and attenuation characteristics as the proposed bus line. The proposed bus line has 30 % smaller line pitch than the conventional co-planar line. Thus, high-speed and high-density bus line can be achieved using the proposed zero-crosstalk structure.

5. Conclusion

We have proposed the novel technique to achieve high-density on-chip bus line using DTLs, and high-density, crosstalk-robust and high-speed bus line structure is shown. The proposed structure can reduce wiring area of 30 % compared with the conventional co-planar line. It is possible to adopt a large number of transmission line interconnects for global interconnects using our structure, and it is expected that high-speed and low-power circuit can be obtained.

References

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[4] H. Ito, *et al.*: IEICE Trans. Electron. **E87-C** (2004) 942.
[5] S. Gomi, *et al.*: *Proc. IEEE CICC* (2004) p. 325-328.
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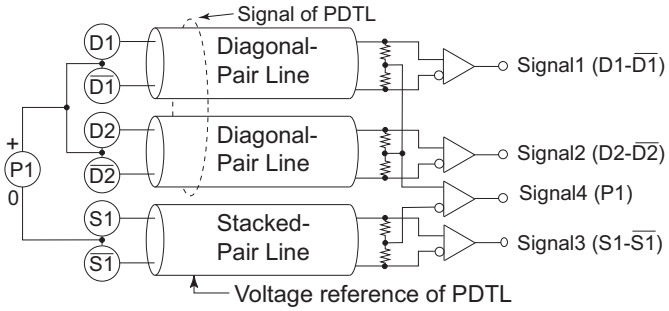

Fig. 1: Schematic of proposed bus line.

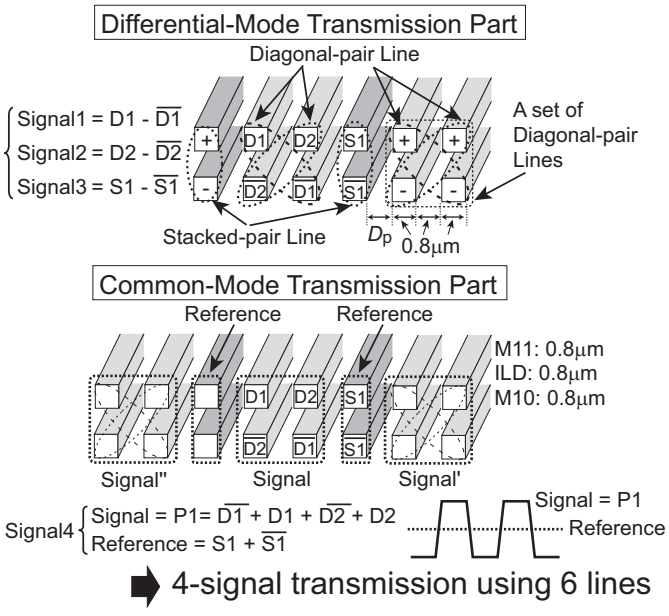

Fig. 2: Cross section of proposed zero-crosstalk bus line structure. DTLs use differential-mode transmission, and PDTLs use common-mode transmission.

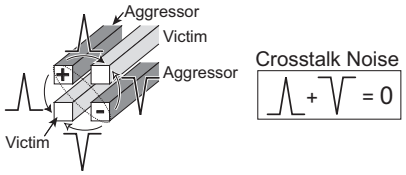

Fig. 3: Principle of noise cancellation.

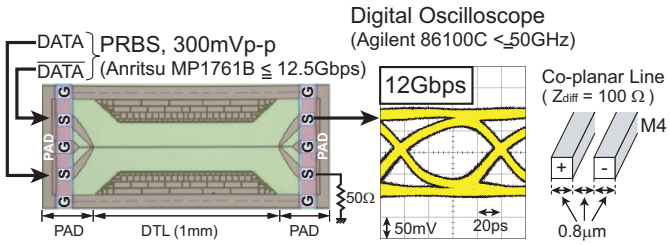

Fig. 4: A chip micrograph of DTL and a time-domain measurement result. The TEG is fabricated using 0.18 μm Si CMOS process. The metal is aluminum. The dielectric is SiO_2.

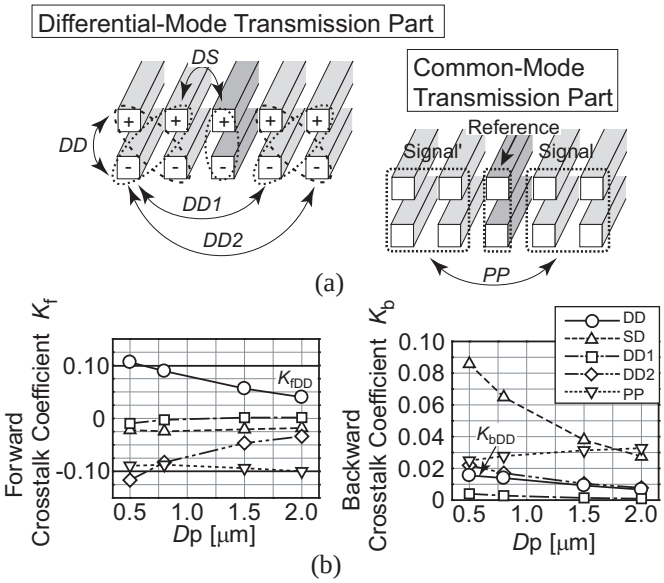

Fig. 5: Crosstalk coefficients between lines.

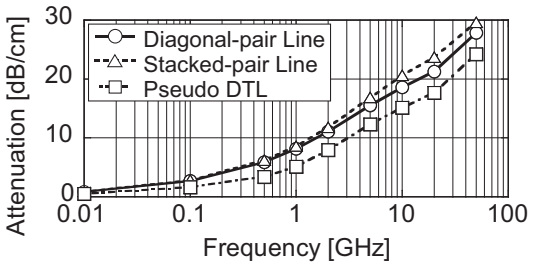

Fig. 6: Attenuation characteristics of DTLs and PDTL.

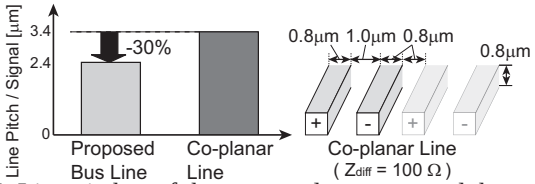

Fig. 7: Line pitches of the proposed structure and the conventional co-planar line.