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Neutron-induced Soft-Error Simulation Technology for Logic Circuits

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1. Introduction

In these years, the interest in soft errors becomes increasing [1]. This comes from the problem that the soft error occurs not only for RAMs but also for logic circuits [2]. RAMs can be robust to soft errors by applying ECC (Error Collection Code). However the ECC can not be applied to logic circuits, soft errors in logic circuits became important.

Because estimation of soft error rates (SERs) is important at the stage of designing circuits, we have developed the SER simulation system to estimate SERs so far [3]-[5]. We have applied this simulation system to the RAMs and have estimated SERs. Moreover, the accuracy of the simulations has been confirmed by carrying out accelerated experiments. In this work, we extended our simulation system to the soft errors in logic circuits. We describe applications for latch circuits and the combinational circuits.

2. Soft error with latch circuits

Soft errors in logic circuits are mainly occurred by secondary cosmic ray neutrons (figure 1) [6]. Figure 2 shows the outline of soft error simulator NISES [3]-[5]. It has the nuclear reaction and the stopping power data base. The nuclear reactions are randomly generated by using the Monte Carlo procedure. When the charged particle penetrates near the p-n junction region and the collected charges exceed the threshold, the soft error occurs. The SER is obtained after repeating these procedures many times. NISES is also applicable for alpha-induced soft errors. Although, we only consider the neutron-SER in this paper, because alpha-SERs are negligible compared with neutron-SERs in logic circuits.

In digital electronics, most of logic circuits consist of combinational circuits and FF circuits. The FF is that temporarily maintains data. The combinational circuit is processing data. Althogh NISES was mainly developed for SER estimations in RAMs, it is also applicable to SER analysis of the latch and FF circuits.

We estimated the SER for a latch circuit with 130nm technology in figure 3 by using NISES. Figure 4 shows the simulated and measured results of SERs for the latch circuit. The accelerated measurement was carried out by using the neutron white beam of Research Center for Nuclear Physics in Osaka Univ. The simulated result agrees well with the measured result as shown in figure 4. The results show that NISES can simulate SER of latch circuits accurately. In the simulated result, the half of soft errors are induced in diode, the others are induced in three nMOSs.

3. Soft error with combinational logic circuits

The mechanism of soft errors in logic circuits is more complicate than those in RAMs. As shown in figure 5, we classified the operating state of a circuit into five states from the viewpoint of the soft error. We assumed that the probability of propagation of the state is described as a certain value. We constructed a simulation system for SER calculations in logic circuits incorporated with SPICE and NISES as is shown figure 6.

The next, we considered latching data at the FF. The FF is only sensitive to the soft error only through a small window around its closing clock edge (Figure 7). We call the time interval of this latching window as the critical time (T_{cri}). T_{cri} depends on size of the noise pulse. We estimated the T_{cri} for each collected charge (Q_0) in the FF with 90nm technology as is shown in Figure 8. The T_{cri} increases as the Q_0 increases because the larger Q_0 gives the larger width of the noise pulse.

To simulate the SER of a chip, it is necessary to simplify the circuit, because of heavy task to estimate all transistors in a combinational logic circuit. A random input is assumed for a logic gate. For a 4-input AND gate, for example, the probability with which a noise pulse propagates through an input is 1/8, where the other three inputs are equal to a logic “1”. We can replace the 4-input AND gate with an inverter with the propagating probability of 1/8. Therefore, a logic circuit can be replaced by an equivalent inverter array as is shown in figure 9.

We estimated the SERs in combinational logic circuits. Figure 10 shows SERs for inverter arrays in equivalent circuits of figure 9, and also shows the sum of the set and hold time (T_{sum}) of FFs. The SER originated by the noise pulse at nMOS is larger than one at pMOS, because of the result as shown in figure 8. When the technology advances, the T_{sum} becomes smaller. Generally, the smaller T_{sum} derives the larger T_{cri} and, the SER becomes increases.

Figure 11 shows the SERs in combinational logic circuits for each single-chip. When the technology advances, the clock frequency and the number of the gate for chip are increases. Hence, SER is getting a severe problem. In the future, presentation of soft errors will become important in logic circuits.

4. Conclusion

We applied soft error simulator NISES for latch circuits and showed that the NISES reproduced the measured result well. We demonstrated the simulation system for SER estimations in combinational logic circuits. The soft error of logic circuits is increasing as the generation advances. In a 45nm generation, it will be necessary to design of logic circuit taking account of soft errors.

Acknowledgement

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[6] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka and N. Matsuoka, IEEE Proc. IEDM Tech. Dig., p. 941, 2004.

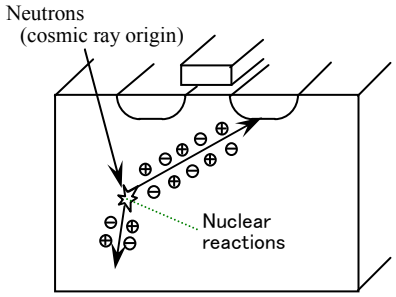

Figure 1 Neutron-induced soft error.

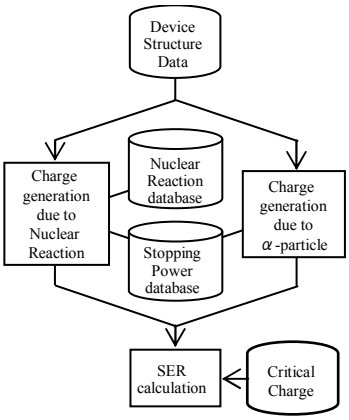

Figure 2 Outline of NISES.

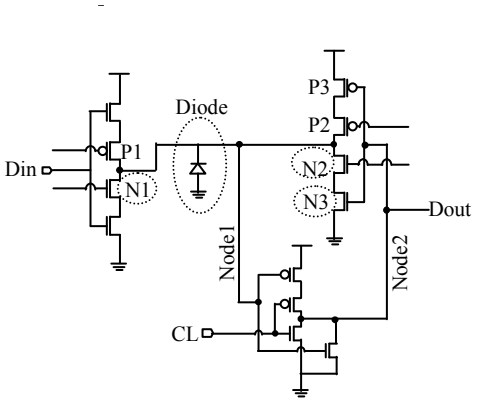

Figure 3 The latch circuit with 130nm technology.

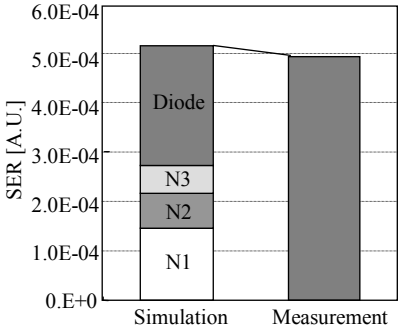

Figure 4 Simulated and measured SERs in the latch circuit with 130nm technology.

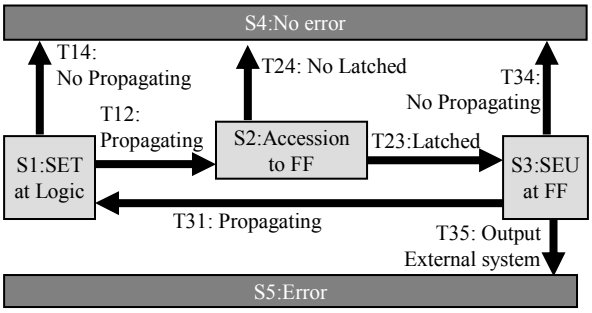

Figure 5 Soft error mechanism in logic circuits.

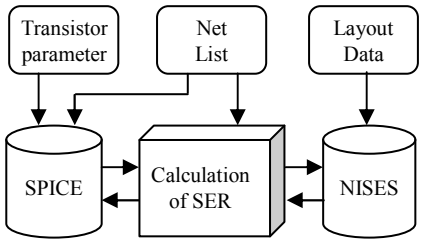

Figure 6 SER Simulation system for logic circuits.

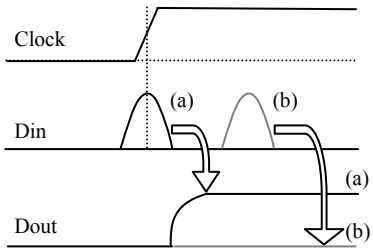

Figure 7 Latching window at data input terminal of an FF: (a) error and (b) no error.

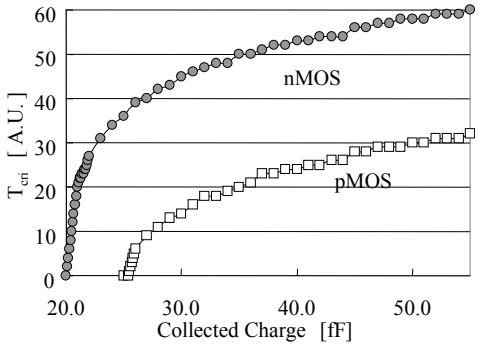

Figure 8 Critical time at data input terminal in a 90nm FF as a function of the collected charge at nMOS and pMOS.

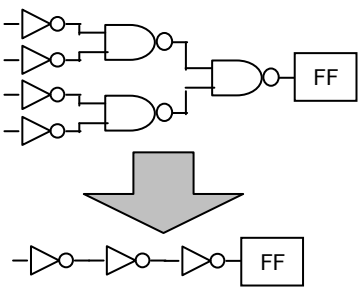

Figure 9. Example of the simplification of a combinational logic circuit.

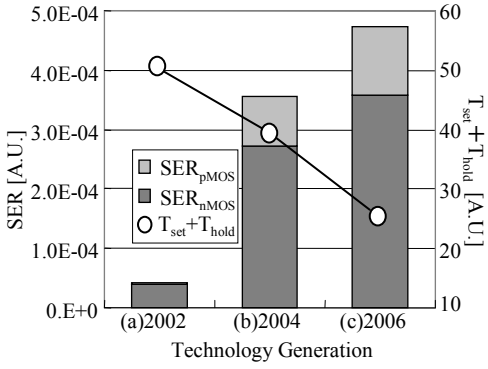

Figure 10. SERs of combinational logic circuits. Technology generation and clock frequency are (a)130nm, 1.3GHz, (b)90nm, 2GHz, and (c)65nm, 3GHz, respectively.

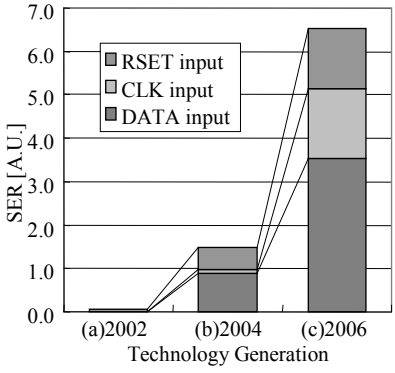

Figure 11. SER/Chip of combinational logic circuits. Technology generation, clock frequency, and total gate number are (a)130nm, 1.3GHz, 5M, (b)90nm, 2GHz, 10M, and (c)65nm, 3GHz, 20M, respectively.