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Mismatches under the Impact of Hot Carrier Stress in 0.15 μm Technology

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1. Introduction

Mismatching properties of MOSFETs on a same wafer are great concerns of both manufacturers and designers, especially when the wafer carrying analog circuits. The mismatches due to process variations are most commonly known [1,2]. Another popular factor being considered is the size effects such as channel length, width, gate area, and layout types [1-5]. However, it is known that HCI (Hot carrier injection) in normal operation will degrade the MOSFET performance, but the mismatches due to this effect have not been fully explored. May be one of the sole example is the reliability mismatches due to HCI on nMOSFETs of one size was reported to having almost the same distribution under different stress voltages [6].

This paper, for the first time, thoroughly presents the hot carrier stress impact on mismatch properties of n and p MOS transistors with different sizes produced using 0.15 μm CMOS technology.

2. Experiments

40 pairs transistors evenly distributed on neighbor hooding 5 dies, half n and half p, on a same wafer were stressed to investigate HCI effects on mismatch properties of these transistors. The HCI stress was performed under maximal substrate current at 25 °C. After each stress period, threshold voltage V_t is monitored at V_{ds}=0.75 V based on constant current method, and I_{ds} was monitored at analog operating condition as gate voltage V_g=V_t+0.3 V with V_{ds}=0.75 V for all nMOSFETs. For pMOSFETs the stress and measurement conditions were the same except that the V_{ds} and V_g were negative biased.

3. Results and Discussion

From Fig.1 and 2, one can observe that, for nMOSFETs, the standard deviations of ΔV_t and $\Delta I_{ds}/I_{ds}$ are enlarged, which means the mismatches are worse after HCI stress. But for the case of pMOSFETs, the changes are much smaller although they possess higher degree of mismatch initially. Also note that the after stress lines of n and pMOSFETs exhibit cross points for both ΔV_t and $\Delta I_{ds}/I_{ds}$ drawings, which mean that the mismatches are the same based on the same gate area. It is suggested that the cross points can be used to indicate the minimal size for n and p pairs to have the same degree of mismatch in designing the devices. For the current case, the minimal gate area should be 0.25μm^2 at $\sigma(\Delta V_t)$ = 8.4 mV when V_t mismatch is the first priority. Similarly, the minimal gate area should be about 0.18μm^2 at $\sigma[(\Delta I_{ds})/I_{ds}]$ = 5% if I_{ds} mismatch is to be considered first. The mismatch shifts after HCI stress and the matching characteristics of n and pMOS transistors are summarized in Table I and Table II, where the A_{Vt} and A_{Ids} in Table II are area factors of corresponding properties defined as [1]

$$\sigma(property) = \frac{A_{property}}{\sqrt{WL}} \quad (1)$$

The statistics reveal that the smallest feature size has the biggest mismatch shift. Hence, the size effect is a dominant factor for property mismatches.

In Fig. 3, 4, 5, and 6, dot lines indicate the trend of property mismatches varying with stress time. It is found that the mismatches of HCI stress degradation on nMOSFETs are more serious than on their counterparts. It is also observed that the degradation rates of properties on nMOS are faster than on pMOS. This can be explained that the HCI stress degrade nMOS matching more heavily than pMOS.

4. Conclusions

The hot carrier injection does degrade matching of nMOSFETs' properties. For pMOSFETs, the changes are minor. It is found that mismatch plots of n and pMOSFETs after stress reveal cross points. The cross points can be used to indicate the minimal size for n and p pairs to have the same degree of mismatches in design phase, such that the circuit performance can be more reliable.

References

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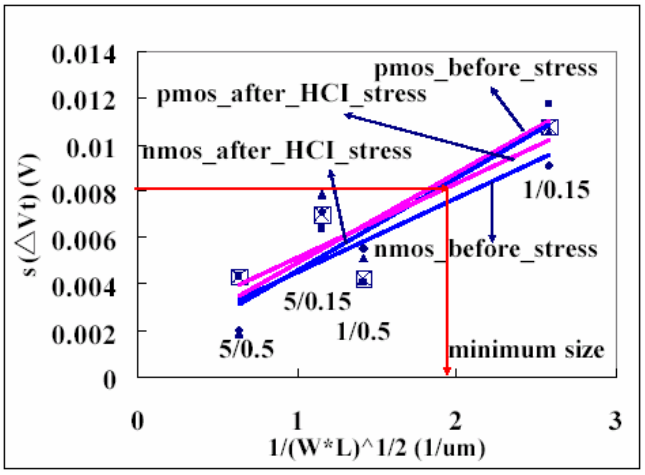

Fig. 1 V_t mismatch versus $1/\sqrt{Area}$

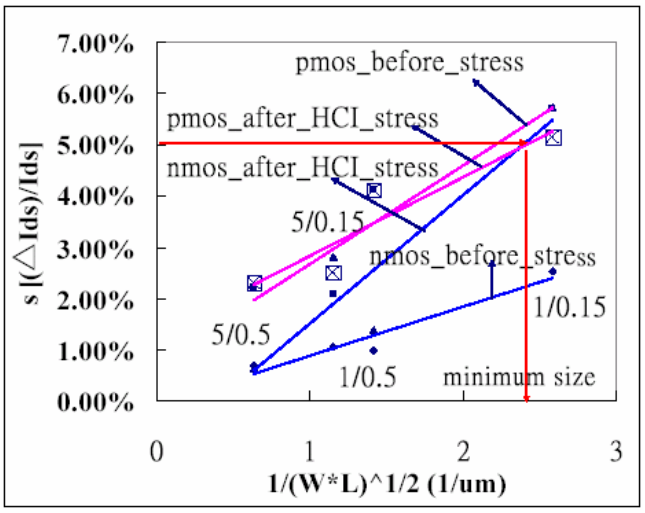

Fig. 2 I_{ds} mismatch versus $1/\sqrt{Area}$

Table I Mismatch shift after HCI stress with multiple W/L ratio

Parameter	Device	Mismatch shift after HCI stress			
		1/0.15	1/0.5	5/0.15	5/0.5
V_t(mV)	nMOS	1.462	-0.41	0.752	-0.15
	pMOS	-1.02	0.144	0.659	-0.013
I_{ds}(%)	nMOS	3.2	0.3827	1.76	-0.035
	pMOS	-0.525	-0.019	0.421	0.0785

Table II Summarized matching characteristics of nMOS and pMOS

Vdd	device	A_{Vt} (mV-μm)	A_{Ids} (%-μm)	Device size
1.5 V	nMOS before stress	0.32	0.96	W/L=1/0.15,1/0.5,5/0.15,5/0.5
	nMOS after HCI stress	0.39	2.5	
	pMOS before stress	0.39	1.92	
	pMOS after HCI stress	0.32	1.53	

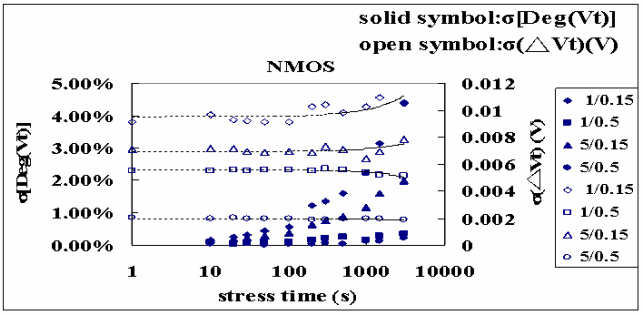

Fig. 3 V_t degradation rate versus stress time with V_t mismatch on nMOS

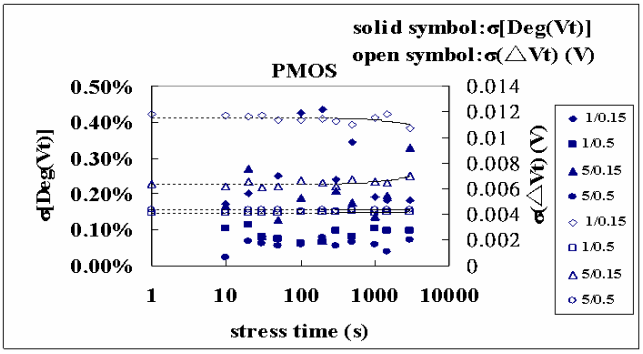

Fig. 4 V_t degradation rate versus stress time with V_t mismatch on pMOS

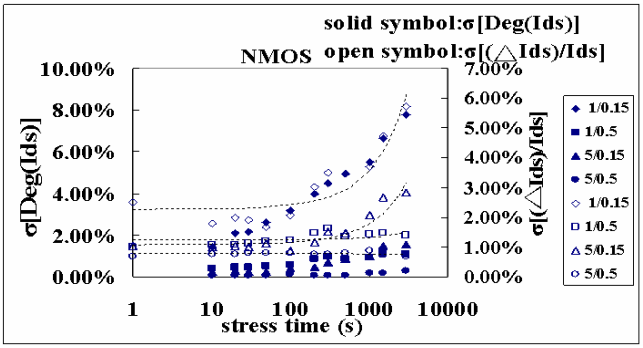

Fig. 5 I_{ds} degradation rate versus stress time with I_{ds} mismatch on nMOS

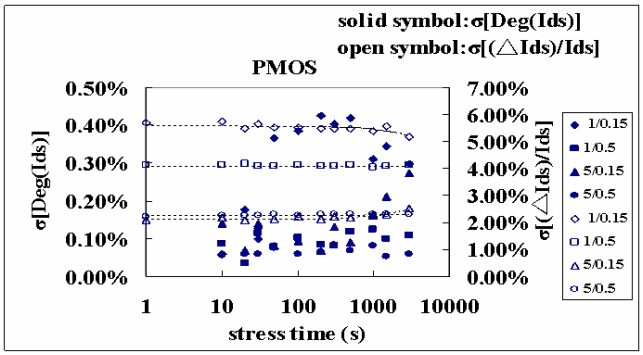

Fig. 6 I_{ds} degradation rate versus stress time with I_{ds} mismatch on pMOS