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E-4-1

Novel Laser Diode Structure consisting of a Si Waveguide and Compound-Semiconductor MQW layers for Si Platform Integration

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1. Introduction

A high-functionality optical device will be required in future high capacity photonic routers for compactness and low cost. A monolithic integration of active devices, such as a laser diode (LD), with Si- or Silica- based planar lightwave circuit (PLC) is very attractive for realizing such a high-functionality optical device.

Compound-semiconductor LDs fabricated on Si substrate using lattice-mismatched heteroepitaxial growth [1, 2] and wafer-bonding [3] techniques have demonstrated continuous-wave (CW) output operations at room temperature (RT). However, since these LDs were fabricated on a planar Si substrate, it would be difficult to connect them to a PLC for monolithic integration. Recently, a Si Raman laser [4] consisting of a Si waveguide has demonstrated a CW output operation at RT. It seems that this laser can be connected to a PLC. However, the laser requires a high optical pumping power of over 200 mW from an external laser, due to the very small Raman amplification efficiency in Si.

In this paper, we propose a novel LD with a core that combines a Si waveguide and compound semiconductor multiple quantum wells (MQWs). The performance of this device, such as its threshold current, is numerically analyzed.

2. Concept of the proposed LD

Figure 1 schematically shows cross-sections of the proposed LD. As shown in Fig. 1(a), this device utilizes a Si waveguide based on silicon-on-insulator (SOI) and consists of a gain region, mode converting regions, and distributed Bragg reflectors (DBRs). In the gain region, as shown in Fig. 1(b), the core consists of Si and compound-semiconductor-based MQWs. The buried oxide layer in the SOI structure is used as a lower cladding layer. Lateral confinement is provided by the air-gap. In order to enlarge the confinement factor at the MQWs, InP is used as the upper cladding layer. Our proposed structure can be realized by using the wafer bonding technique [3].

3. Design of the device

The confinement factor in the gain region is one of the important parameters for designing a LD. Figure 2(a) shows the detailed structure of the proposed LD, which was used in calculating the mode field profile and confinement factor. The structure consists of Si substrate, a 500-nm-thick SiO_2 lower cladding layer, a Si core with height, h_{Si}, and width, w_{Si}, a 150-nm-thick InP spacer, a 50-nm-thick unstrained 1.3Q-InAlGaAs separated confinement heterostructure (SCH) layer, a strain-compensated InAlGaAs MQWs, a 50-nm-thick unstrained 1.3Q-InAlGaAs SCH layer, and an InP upper cladding layer. The MQW layers consist of 5 sets of a 70-nm-thick InAlGaAs well with compressive strain (0.85%) and a 100-nm-thick InAlGaAs barrier with tensile strain (-0.55%). The barrier layers have a band gap corresponding to a wavelength of 1.3 μm.

Figure 2(b) shows calculated confinement factors for the Si core and MQW layers. Here, the confinement factor for the MQWs includes that for both the well and barrier layers. As the width or height of the Si core increases, the confinement factor for the MQW layers decreases while that for the Si core increases. The factor of 1%/well (corresponding to 13 % for the MQW layers) is similar to that of conventional compound-semiconductor based LD. This value can be achieved at h_{Si} of 0.7 μm and w_{Si} of 0.7 μm in our proposed structure (filled circle in Fig. 2(b)). This small Si core can be fabricated using conventional stepper-based photolithography and dry-etching techniques.

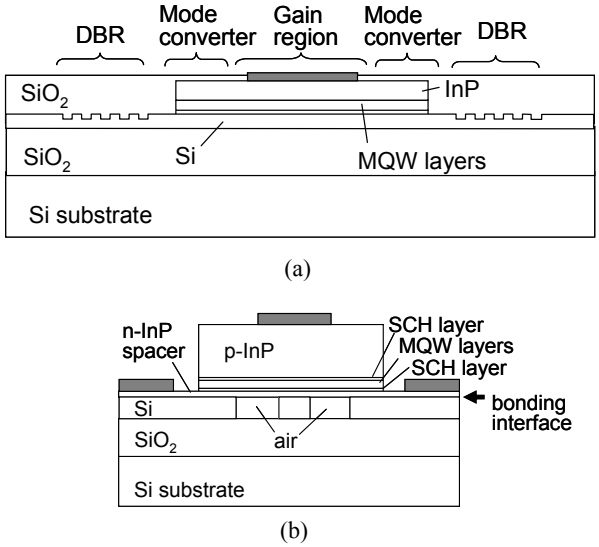
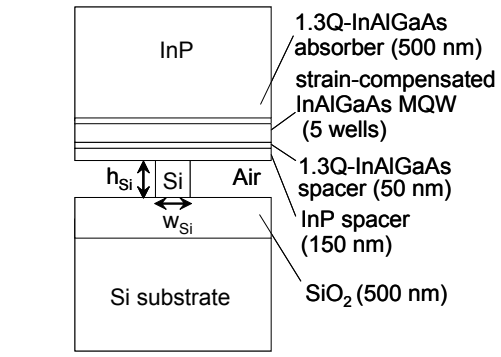
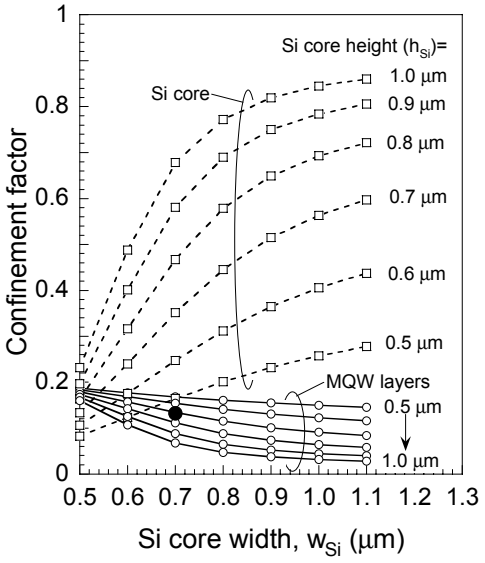


Fig. 1 Schematic cross-section of the (a) whole structure and (b) gain region of the proposed LD.

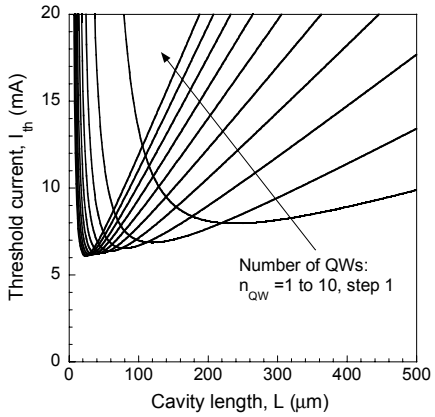


(a)

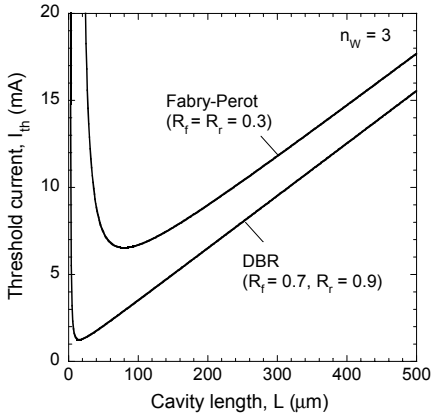


(b)

Fig. 2 (a) Detailed schematic cross-sectional structure in the gain region of the proposed LD and (b) calculated confinement factors for the Si core and MQW layers.



(a)



(b)

Fig. 3 (a) Calculated threshold currents as a function of cavity length for a Fabry-Perot LD with proposed the structure. (b) Comparison of the threshold currents between the Fabry-Perot and DBR LDs.

3. Threshold Current

Figure 3(a) shows the calculated threshold current, I_{th}, of a Fabry-Perot LD with cleaved facets as mirrors. The cross-sectional structure of the gain section is the same as that in Fig. 2(a). The calculated gain of the MQWs was 5000 cm^{-1}/well at a wavelength of 1.55 μm with a sheet carrier density of 3 x 10^{12} cm^{-2}. Internal quantum efficiency and internal loss were assumed to be 0.8 and 15 cm^{-1}, respectively, which are the values used for conventional compound-semiconductor-based LDs. The confinement factor and mode field width at the MQWs were 1 %/well and 5 μm. These values were obtained from the calculation of the mode filed profile. The reflectivity of the front and rear mirrors (R_f, R_r) was set to 0.3. As shown in Fig. 3(a), the minimum I_{th} decreases as the number of QWs, n_{QW}, increases. For example, at a cavity length, L, of 80 μm and n_{QW} of 3, the I_{th} is calculated to be 6.5 mA.

The I_{th} can be further decreased by using high reflection-mirrors such as DBRs. Figure 3(b) shows the calculated I_{th} for the LD with DBRs (R_f = 0.7 and R_r = 0.9). The n_{QW} is 3. For comparison, the I_{th} for Fabry- Perot type LD is also plotted in Fig. 3(b). As shown in Fig. 3(b), the I_{th} at L of 80 μm can be decreased to 2.9 mA. This value is as small as that of well-designed compound-semiconductor LDs with CW output operation. These results indicate that the proposed structure is highly promising for realizing LDs on Si PLCs.

4. Conclusions

We have proposed a novel laser diode (LD) with a core combining a silicon waveguide and InAlGaAs MQWs. Calculation results shows that the proposed LD with DBR mirrors has a very small threshold current of less than 3 mA at a cavity length of 80 μm. The proposed LD is very promising for realizing integrated Si photonics device.

References

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