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A 51,272-gate-count Dynamic Optically Reconfigurable Gate Array in a standard 0.35μm CMOS Technology

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I. Introduction

High-speed reconfigurable processors have been developed in recent years: DAP/DNA chips and DRP chips [1][2]. These devices can be changed from one context to the other context at every clock cycle in a few nanoseconds. However, the die size limits the number of reconfiguration contexts of currently available DAP/DNA and DRP chips to 4-16.

In contrast, Optically Reconfigurable Gate Arrays (ORGAs) [3][4] can easily enable both fast reconfiguration and numerous reconfiguration contexts using an optical holographic memory and optical wide-band reconfiguration connections. Such devices present the possibility of large virtual gate-count VLSIs.

However, even though the virtual gate-count is extremely large, a high real gate-count is required to increase the amount of the working circuit at any moment. Therefore, we have already proposed dynamic optical reconfiguration circuit that is the smallest optical reconfiguration circuit among all ORGAs; we continue the development of high-gate-count Dynamic ORGAs (DORGAs) [5].

This paper presents a new design of a 51,272-gate-count DORGA modified from a previously designed 26,350-gate-count DORGA [6] using standard 0.35 μm four-metal CMOS process technology.

II. Optical Reconfiguration Circuit

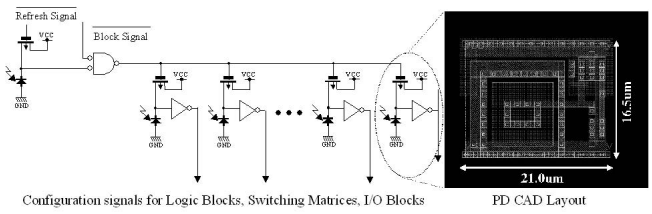

Fig. 1. Schematic diagram of an array of optical reconfiguration circuits and CAD layout of a photodiode cell including a photodiode and an optical reconfiguration circuit.

We have proposed a dynamic optical reconfiguration circuit that eliminates the static memory function of the VLSI part and uses dynamic method, as shown in Fig. 1 [5]. In the circuit, the gate array information is stored in photodiodes instead of latches, flip-flops, or memory. Photodiodes not only detect light, but also serve as dynamic memory. The photodiode states are connected directly through inverters to the gate array portion.

TABLE I
Specification of a high-density DORGA.

Technology	0.35 μm double-poly 4-metal CMOS process
Chip size	14.2 $\times$ 14.2 [mm]
Supply Voltage	Core 3.3 [V], I/O 3.3 [V]
Photodiode size	9.5 $\times$ 8.8 [μm]
Distance between Photodiodes	h.=28.5-42 [μm], v.= 12-21 [μm]
Number of Photodiodes	170,165
Number of Logic Blocks	1,508
Number of Switching Matrices	1,589
Number of I/O bits	272
Gate Count	51,272

III. Gate Array Design

A new 51,270-gate-count DORGA-VLSI chip was designed using a 0.35 μm standard CMOS process. Table 1 shows those specifications. The acceptance surface size of the photodiode and photodiode-cell size, including an optical reconfiguration circuit, are 8.8 μm $\times$ 9.5 μm and 21.0 μm $\times$ 16.5 μm, respectively. The photodiodes were constructed between N+ diffusion and the P-substrate. The photodiode cells are arranged at 28.5-42.0 μm horizontal intervals and at 12.0-21.0 μm vertical intervals; 170,165 photodiodes are used. The fourth metal layer is used for guarding transistors from light irradiation; the other three layers were used for wiring. The gate array portion was designed using Design Compiler and Apollo (Synopsys Inc.), respectively, as the logic synthesis tool and the place and route tool.

Fig. 2 shows a block diagram of an Optically Reconfigurable Logic Block (ORLB). The ORLB consists of two four-input Look-Up Tables (LUTs), multiplexers, two D-flip flops, and tri-state buffers, along with the structure of FPGAs. A point of difference from FPGAs is that all states of the LUTs,

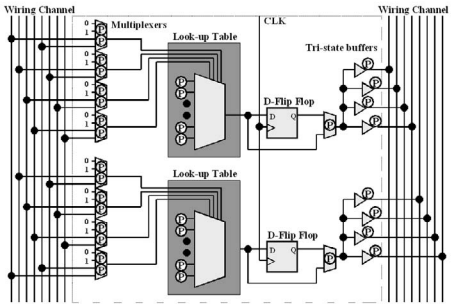

Fig. 2. Block diagram of an Optically Reconfigurable Logic Block (ORLB).

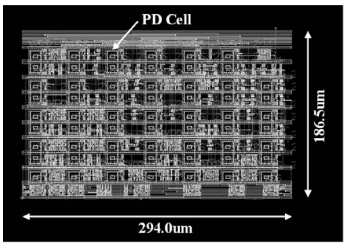

Fig. 3. CAD layout of an Optically Reconfigurable Logic Block (ORLB).

multiplexers, and tri-state buffers are optically programmable through 58 photodiodes. One optical reconfiguration circuit is added to an ORLB as a block reconfiguration assignment. Therefore, 59 photodiodes are used in the ORLB. The CAD layout is shown in Fig. 3. The cell size is 294.0 μm $\times$ 186.5 μm. Wiring was executed using the first to the third metal layers while avoiding the aperture area of the photodiode cell.

Fig. 5 shows a block diagram of an Optically Reconfigurable Switching Matrix (ORSM). The ORSM structure is fundamentally identical to that of units sold by Xilinx Inc., but each transmission gate is controlled by an optical reconfiguration circuit. Fig. 6 shows the CAD layout. The cell size is 177.0 μm $\times$ 186.5 μm. As with the ORLBs, wiring was executed using only the first and second metal layers, avoiding the aperture area of the photodiode cell. Finally, Fig. 4 shows the CAD layout of a part of entire gate array; the ORLB and ORSM are placed alternately in the horizontal direction.

The reconfiguration speed of the dynamic reconfiguration circuit used for this implementation was measured using a fabricated chip with the same photodiode structure. Experimental results confirmed the photodiode response time as less than 4 ns. In the case that the pulse-wide refresh to charge junction capacitance is 1 ns, the reconfiguration cycle is executable in less than 5 ns.

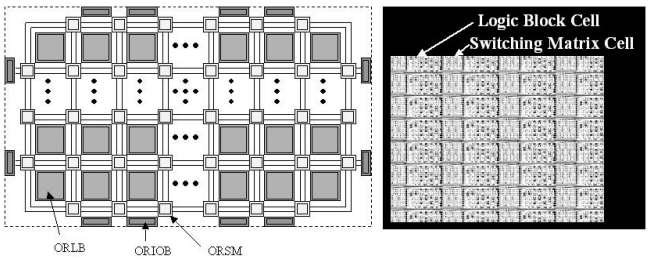

Fig. 4. Block diagram and CAD layout of a part of an entire gate array.

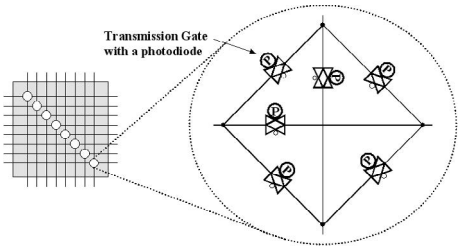

Fig. 5. Block diagram of an Optically Reconfigurable Switching Matrix (ORSM).

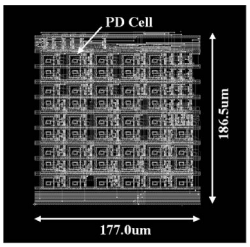

Fig. 6. CAD layout of an Optically Reconfigurable Switching Matrix (ORSM).

IV. Conclusion

This paper presented the design of the largest 51,272-gate count ORGA using 0.35 mm four-metal CMOS technology. Furthermore, we have confirmed that the reconfiguration cycle is executable in less than 5 ns. In the near future, this design will be fabricated.

V. Acknowledgments

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