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E-5-2

Reduction of Random Noise for CMOS Image Sensors with 2.2μm×2.2μm Pixel

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1. Introduction

CMOS image sensor is a key device as an electrical eye for the ubiquitous era. Mega-pixel CIS for mobile device is already available in a consumer market, and the application is becoming broader. It is expected the unit pixel size down to 2x2 um^2 or smaller to emerge a few years. Especially noise characteristics become a critical factor as pixel size scales down, and it should be improved to maintain high dynamic range (20log(saturation/noise)) with scaling which is a key figure of merit of image sensor, since saturation level tends to be degraded with smaller pixel size. In CIS, one of major noise sources is flicker noise originated from source follower transistors of pixels. It is well known that the flicker noise is strongly dependent on the interface quality of gate oxide and SiO2 gives better interface compared with any nitride oxides. Because logic devices co-integrated with CIS pixels require relatively highly nitrided-oxide for suppressing boron penetration, gate oxide process should be optimized for satisfying both pixel devices (all NMOS) including source followers and logic devices. This paper addresses some distinct process approach for the 2.2 x 2.2 um^2 pixel CIS with low noise characteristics, which includes (1) adopt of plasma nitride oxide and (2) dummy heat treatment. Based on our knowledge, the above approach for CIS is first reported in this work.

2. Device fabrication and characteristics

1.3M(SXGA) CIS chips with 2.2 x 2.2 um^2 pixel size were fabricated using a modified 130 nm technology which adopts 90nm technology for pixel and 130nm technology for logic. Fig.1 is a schematic diagram of one pixel with 4-transistors. Some key figures of merit of a fabricated CIS chip are listed in the Table.1. Good dynamic range (good noise characteristics) was obtained without sacrificing other major characteristics. This work will addresses key approaches for reducing noise of CIS. To investigate the effect of gate oxide interface on noise, some experiments were applied:

(1) Dummy heat annealing

As shown in Fig.2, dummy heat (800°C 30~60m) annealing after gate formation reduces 1/f (flicker) noises. This result can be attributed to curing effect during annealing. To confirm the effect of 1/f noise characteristics to the CIS output, the random noise was measured for the fabricated chips under dark illumination. Noise characteristic confirms the effect of dummy heat annealing (Fig.3).

(2) Gate nitridation methods

Next, gate oxide was changed. Fig.4 compares 1/f noise between the conventional NO(nitride oxide) gate and SiO_2 (pure oxide) gate. The NO gate shows poorer 1/f noise than SiO_2, which indicates the increment of nitrogen concentration in Si-oxide interface degrades the trap density [2]. So, when it comes to gate oxide for CIS with small pixel, different nitride concentration is needed for pixel and logic devices: low nitride concentration in Si-oxide interface for pixel (good 1/f noise) and high nitride concentration for logic devices with thin gate oxide (suppression of boron penetration). For the purpose of obtaining nitrided layer imposing little influence on the oxide-Si interface for pixel devices, the surface plasma nitridation (PN) technique was applied. It was confirmed that nitrogen of PN oxide is locally located at the top surface of oxide by SIMS. Fig.5 compares the interface trap density for three different gate oxides: NO gate(no heat), PN gate(no heat), and PN gate + dummy heat. It is clear PN gate has lower interface trap density than NO gate. Fig.6 compares the measured random noise characteristics for the three samples. The sample with PN gate + dummy heat annealing shows the best noise characteristics. From the above results, it can be concluded that random noise can be reduced to the level of pure SiO_2 by using the PN process. Because additional heat treatment for pixel devices can aggravate boron penetration of PMOS logic device, dummy heat effect on threshold shift of NO oxide and PN oxide was compared. As shown in Fig.8 PN oxide does not show Vt shift, whereas NO oxide shows higher Vt shift, indicating boron penetration.

Conclusion

1.3M (SXGA) CIS chips with pixel size as small as 2.2 x 2.2 um^2 with improved noise characteristic are successfully implemented by applying dummy heat annealing and plasma nitride (PN) oxide process. PN oxide also shows better immunity against boron penetration compared to the conventional NO gate when dummy heat treatment is applied.

References

[1] S K. Mendis, et al., IEEE J. of Solid-State Circuits, p187, 1997.

[2] T. Ohguro, et al., Symp. VLSI Tech., p.37, 2003.

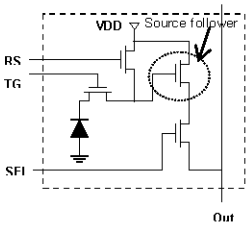

Fig.1. Schematic circuit diagram of one pixel consisting of 4-transistors

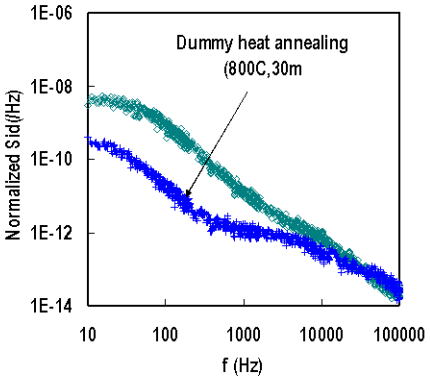

Fig.2 The effect of dummy heat annealing (800°C, 30m) on 1/f (flicker) noise characteristic. (NO gate was applied in common)

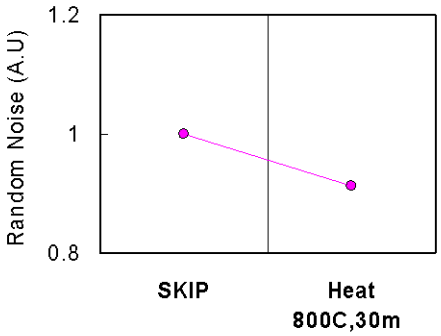

Fig. 3 Comparison of random noise characteristics from the fabricated CIS chip. Dummy heat (800°C, 30m) treatment shows improved random noise characteristics. (NO gate was applied in common.)

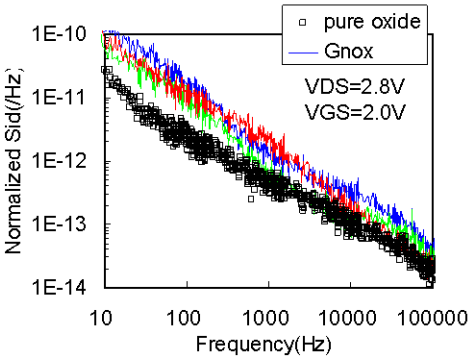

Fig. 4 1/f (flicker) noise comparison of SiO2 gate and conventional nitride oxide (NO, or Gnox) NMOS transistor.

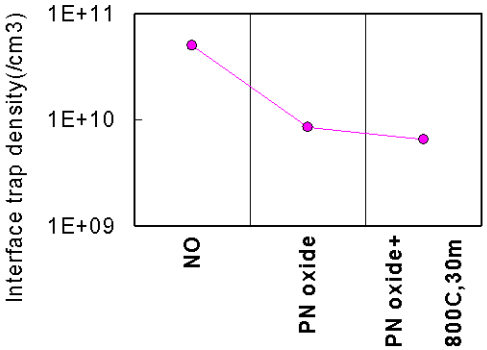

Fig. 5 Comparison of interface trap density measured by charge pumping method for three samples: NO gate (without dummy heat), PN gate, and PN+ dummy heat annealing. PN oxde shows lower interface trap density than the conventional NO gate.

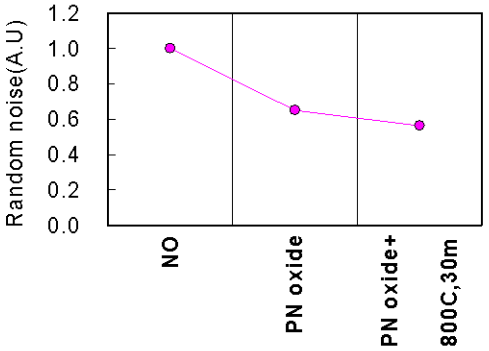

Fig. 6 Comparison of random noise characteristics for three samples. PN oxide shows better RN than NO gate.

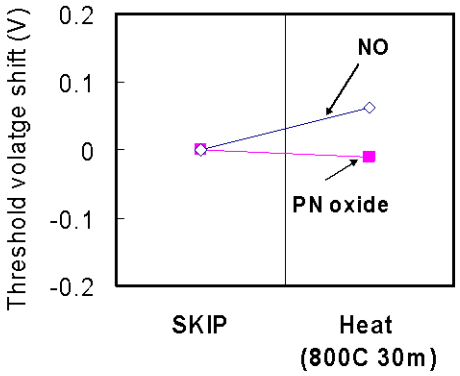

Fig. 7 Comparison of threshold shift of PMOS transistors with PN oxide and the NO gate when dummy heat (800°C,30m) is applied. PN oxide shows higher immunity against the boron penetration than the NO gate.

Pixel pitch	2.2 um
Sensitivity	1500mV/lux.sec
Saturation level	700mV
Dark level	< 20mV/sec @60°C
Dynamic range	> 60 dB
Image lag	free

Table.1 Key figures of merit of a fabricated CIS chip (without color filter