Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.990-991

F-10-5

Improvement of on/off ratio of pentacene static induction transistor with ultra-thin CuPc layer

Yasuyuki Watanabe[1], Hiroyuki Iechi[1, 2] and Kazuhiro Kudo[1, 3]

[1]Optoelectronic Industry and Technology Develepment Association, Advanced Organic Device Project, Chiba Laboratory
1-33 Yayoicho, Inage-ku, Chiba, 263-8521, Japan
Phone: +81-43-290-3246 E-mail: watanabe@restaff.chiba-u.jp
[2]Advanced Technology R&D Center, Research and Development Group, Ricoh Co. Ltd
16-1 Shinei, Tsuzuki, Yokohama 224-0035, Japan
[3]Department of Electronics and Mechanical Engineering, Faculty of Engineering, Chiba University
1-33 Yayoicho, Inage-ku, Chiba, 263-8521, Japan

1. Introduction

Organic field effect transistors (OFETs) are very attractive device for fabricating the flexible displays, information tags, etc. However, organic semiconductors have some disadvantages of low current density and low speed of operation due to their high resistivity and low carrier mobility.

Organic static induction transistor (SIT) with vertical structure has been expected for the high-speed and high-power operation device [1] due to the short channel length than that of lateral type transistor such as metal-oxide-semiconductor transistors (MOSFETs).The excellent characteristics of the organic SIT arise from the very short length corresponds to the thickness of an organic semiconductor film between the source and drain electrodes. The gate electrode is inserted into the semiconductor layer. In our past research, organic SIT using CuPc thin film and Au source electrode was fabricated on glass substrate and the dynamic characteristics showed a cutoff frequency of 2.3 kHz [2]. However, the organic SIT has problems such as low on/off ratio and low current value.

In this study, to achieve the high on/off ratio and high current values in the organic SIT, we studied the influence of inserting ultra-thin CuPc layer between the source electrode and pentacene film on the static characteristics of organic SIT.

2. Experimental procedure

Figure 1 shows a schematic diagram of a pentacene SIT. Device processing is as follows. First, the ultra-thin CuPc layer of 1 nm was deposited on ITO formed on glass substrete. Second, the pentacene thin film of 100 nm was deposited on the CuPc layer. Third, a very thin Al film of 30 nm was formed on the pentacene film. It was found that the characteristics of the SIT were greatly affected by a very thin Al film. The ideal Al gate electrode should be of the mesh type [1],[3]. In this experiment, a grid type gate electrode with a line and space region was fabricated using an evaporation mask. The thicker Al part of the grid gate blocks the current flow from the source to the drain electrode due to the formation of double Schottky barriers, and the wider gap region of the gate electrode also does not control the current flow effectively [1]. The dimension and edge feature of evaporated Al electrode are controlled by adjusting the evaporation material source size, the distance between the source and the substrates, and the space between the substrate and the evaporation mask. In this case, the estimated the gap between gate electrodes was approximately 4 μm. Fourth, the Al film as a gate electrode was covered with the pentacene film of 100 nm. Finally, the drain Au electrode was formed on the pentacene film. The CuPc layer and pentacene films were fabricated under a vacuum of 2×10^{-4} Pa. The source temperature of CuPc and pentacene were approximately 200℃ and 420℃, respectively. The evaporation rate of organic semiconductors were 0.1nm/s.

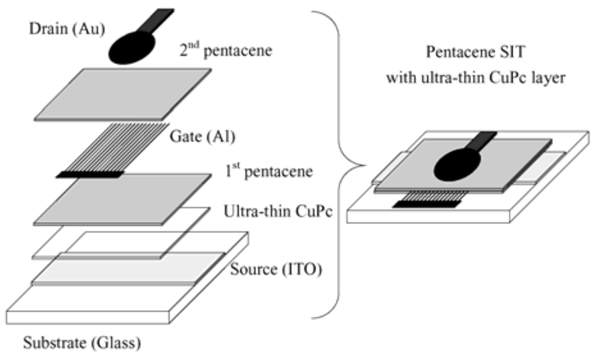

Fig. 1. Schematic diagram of pentacene SIT with ultra-thin CuPc layer on glass substrate.

3. Results and discussion

Figure 2 and 3 show the static characteristics for the pentacene SIT with and without an ultra-thin CuPc layer. In both samples, drain-source current (I_{DS}) at a constant drain-source voltage (V_{DS}) decreases with increasing gate voltage (V_G). This phenomenon demonstrates that the majority carriers of holes in the pentacene flow from the source to the drain and are controlled by gate voltage V_G applied to the Al Schottky gate electrode. From these results, the on/off ratio and the current value for the SIT with an ultra-thin CuPc layer were higher than those for the SIT without an ultra-thin CuPc layer. On the other hand, from Fowler-Nordheim tunneling theory[5], an equation mentioned bellow was obtained.

$$I_{DS} \propto V_{DS}^{\ 2} \exp\left(\frac{-\kappa}{V_{DS}}\right)$$

where κ is a parameter that depends on the barrier shape.

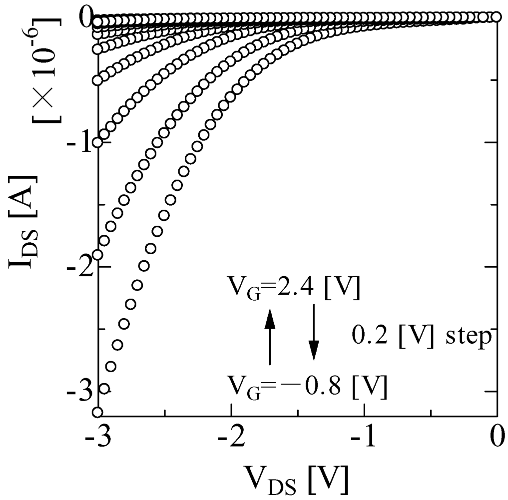

Fig. 2. Static characteristics of the pentacene SIT with an ultra-thin CuPc layer.

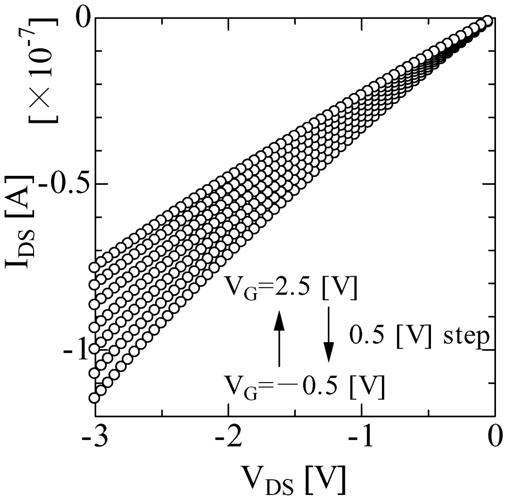

Fig. 3. Static characteristics of the pentacene SIT without an ultra-thin CuPc layer.

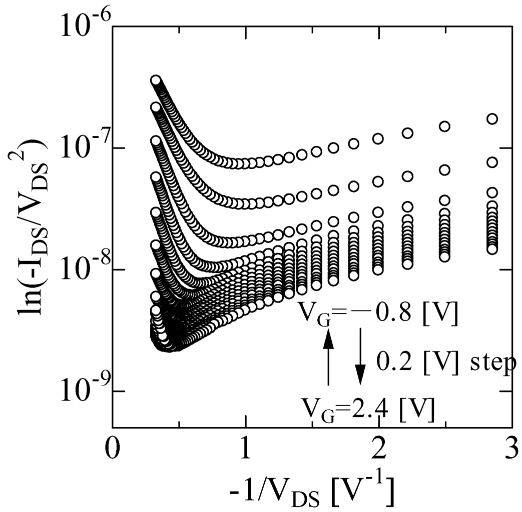

Fig. 4. Fowler-Nordheim plot of the static characteristics for the pentacene SIT with an ultra-thin CuPc layer.

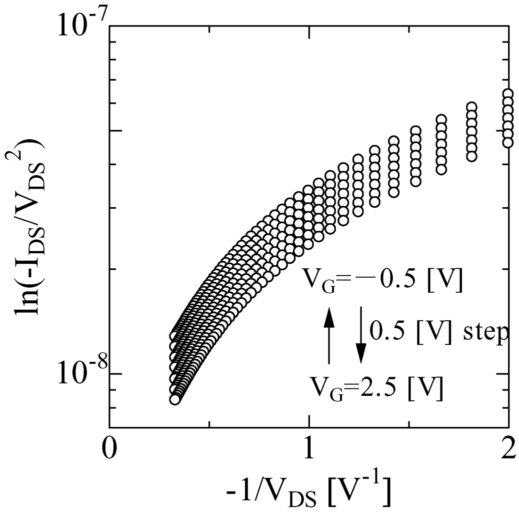

Fig. 5. Fowler-Nordheim plot of the static characteristics for the pentacene SIT without an ultra-thin CuPc layer.

Figure 4 and 5 show ln($-I_{DS}/V_{DS}^2$) vs $-1/V_{DS}$ characteristic known as Fowler-Nordheim plot (FN plot)[6] of the static characteristics for the pentacene SIT with and without an ultra-thin CuPc layer. They were characterized to conform the dependence of the gate voltage V_G on the tunneling current in drain-source current I_{DS}. If the gradient is negative, the tunneling current were contained in drain-source current I_{DS}. In case of the plot for the SIT with the ultra-thin CuPc layer, deviation from the negative gradient at higher V_{DS} is likely to be due to the tunneling current.

These results demonstrate that the formation of the hole injection barrier at the pentacene / ITO interface is effective to fabricate the high performance organic SITs.

3. Conclusions

We found that there was clear correlation between the modulation in static characteristics of a pentacene SIT and an interface condition of organic semiconductor layer / source electrode. As a result, it is necessary to form the hole injection barrier on a source electrode to achieve the high on/off ratio and high current value for the organic SIT. The barrier works effectively as controlling a tunnel current from a source electrode by applying the gate voltage.

Acknowledgements

A part of this work belongs to “Advanced Organic Device Project” which OITDA contracted with New Energy and Industrial Technology Development Organization (NEDO).We would like to thanks to all the members of the Advanced Organic Project in Chiba Laboratory for fruitful discussions.

References

[1] K. Kudo, D. X. Wang, M. Iizuka, S. Kuniyoshi and K. Tanaka, Thin Solid Films **331** (1998) 51.

[2] D. X. Wang, Y. Tanaka, M. Iizuka, S. Kuniyoshi, K. Kudo and K. Tanaka, Jpn. J. Appl. Phys **38** (1999)256.

[3] D. X. Wang, M. Iizuka, S. Kuniyoshi, K. Kudo and K. Tanaka, Trans. IEE. J. A **118** (1998) 1166.

[4] K. Kudo, M. Iizuka, S. Kuniyoshi and K. Tanaka, Thin Solid Films **393** (2001) 362.

[5] R. H. Powler and L. Nordheim, Proc. R. Soc. London Ser. **A119** (1928) 173.

[6] I. D. Parker, J. Appl. Phys **75** (1994) 1658.