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Creation of Strained and Relaxed SiGe films simultaneously through Ge condensation on SOI

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1. Introduction

Complementary metal oxide Semiconductor (CMOS) transistors on high mobility channel materials such as strained Si on insulator provide an evolutionary path to highly scaled, low supply voltage, integrated circuits.[1] Ge condensation is one attractive technique which allows realization of SiGe on insulator.[5] From device perspective, compressively strained SiGe is a promising candidate for p-MOS due to high effective hole mobility in such film. On the other hand, tensile strained silicon can provide high electron mobility in n-MOS. Such tensile strained Si can be grown on a relaxed layer of SiGe .[1-3] Thus it is highly desirable that a processing scheme is identified to form relaxed SiGe as well as compressive SiGe on insulator (SGOI) on the same wafer for n-MOS and p-MOS fabrication respectively.

Among different techniques available, to achieve relaxation in SiGe films,[4,5] thicker initial SiGe layers and higher oxidation temperatures have shown higher relaxation rate and lower dislocation density, respectively.[6] It has been also found that the mesa isolation of SiGe/SOI structures into small active areas yield larger relaxation of the SGOI layer after oxidation.[7] Tezuka, et al have also indicated that it is possible to achieve relaxed and compressive SiGe on insulator, though most device data published are on p-MOSFET on compressive SGOI. Our objective in this work is to obtain relaxed SiGe which is suitable for growing strained Si for n-MOSFETs and compressive SiGe which is suitable for p-MOSFETs on insulator with same process conditions so that ultimate CMOS integration is viable. We have also identified the factors which lead to surfaces with low number of pit-defects and reduced surface roughness.

2. Experimental Approach

$Si_{(0.85)}Ge_{(0.15)}$ of thickness 130 nm was deposited on SOI substrates using Ultra High Vacuum Chemical Vapour Deposition (UHVCVD) technique. This thickness is kept below the critical thickness at deposition temperature in order not to generate misfit dislocations at this stage. SOI wafers have a starting silicon thickness of 35 nm. Mesa structures were patterned and etched with the etch stopping on the buried oxide layer of SOI wafer. Some portions of the wafer were preferentially etched by masking to reduce the thickness of SiGe selectively. The etching was performed in a HBr and Cl based chemistry down to 90 nm thickness in these selected mesa regions. After subsequent photoresist strip and polymer removal steps, these wafers were subjected to cyclic oxidation and annealing steps at high temperature to condense the Ge to higher fractions. Figure 1 shows the calculated thickness and Ge concentrations,[8] for different starting SiGe thickness (SiGe1=130 nm, SiGe2=90 nm) after different lengths of condensation process measured in terms of SiGe thickness reduction with oxidation. We exploit the difference in concentration to achieve the specific goals for p-MOS and n-MOS. It can be predicted from Figure 1 that at a SiGe thickness of 65 nm, with a starting thickness of 130 nmon 35 nm thick SOI, the Ge concentration will be 30 %. The corresponding concentration with SiGe thickness of 25nm (starting thickness 90 nm), will have a Ge concentration of 54%. The condensation process was tailored to achieve these values simultaneously. It is presumed here, to a first order approximation that the Si consumption rate is the same for both the thicknesses. x1 and x2 correspond to the Ge fractions in SiGe1 and SiGe2 respectively. As demonstrated by the results here, a higher starting thickness leads to relaxation of SiGe layer while a lower starting thickness conserve the compressive strain under same processing conditions. The samples were subsequently analyzed for strain, SiGe thickness, Ge concentration, defects, and surface roughness.

3. Results and Discussion

We first identified process conditions which lead to pitting-free SGOI layers. For instance, condensation without pre-anneal leads to a pit density of roughly around 10 pits per 100 square microns (Fig. 2A). A pre-anneal treatment before Ge condensation results in a pit-free surface (Fig. 2B).

The thickness of the resulting SiGe layer was obtained from TEM cross sections as shown in Fig. 3. The TEM cross sections revealed a SiGe thickness of 74.7 nm, for SiGe1 and 12.8 nm for SiGe2. The cross sections also show single crystal nature of the layers without any observable defects. The thicker sample showed a uniform composition of 20% while the thinner sample showed a composition of 45% as measured using EDX.

Strain analysis was done using micro Raman analysis and high resolution XRD. It can be clearly seen from Figure 4 that the thicker sample from SiGe1 is fully relaxed with the Si-Si phonon peak from SiGe layer at 508 cm^{-1} (at 20% Ge). At the same time, the thinner sample from SiGe2 showed a blue shift indicating a compressive strain. XRD analysis from SiGe1 showed a cubic lattice with lattice parameter ~ 5.475 Å in all three directions (Fig. 5). This confirms relaxation as indicated by Raman spectra. XRD signals from SiGe2 indicate a compressive strain. These techniques confirm that both

strained and relaxed SiGe layers are obtained with same processing conditions.

Both types of SiGe layers exhibited low surface roughness as measured using AFM (Fig. 6). The RMS roughness of 0.34 nm and 0.25 nm were obtained on relaxed SiGe and compressive SiGe respectively. Also one can clearly observe the cross-hatch pattern on relaxed SiGe, but no such pattern on compressive SiGe.

4. Conclusion

We have obtained relaxed SiGe which is suitable for growing strained Si for n-MOSFETs and compressive SiGe which is suitable for p-MOSFETs on insulator with same process conditions. We have also identified the factors which lead to surfaces with low number of defects and reduced surface roughness.

References :

1 C.W Leitz, et.al., J.Appl. Phys. 92, 3745 (2002).
2 R.Koh, Jpn. J. Appl. Phys., 39, 2229 (2000)
3 C.O.Choi, et.al. IEEE Electron. Device Lett., 23, 473 (2002).
4 S.Kawano, et al., Appl. Phys. Letters, 85, 2514 (2004).
5 S. Takagi, et. al., Appl. Sfc. Science, 224, 241 (2003).
6 N. Sugiyama, et. al., Ext. Abstracts of the Conference on Solid State Devices and Materials, vol. 146, 2002.
7 T. Tezuka, et. al., Appl. Phys. Lett. 80 (2002) 3560
8 T.Tezuka, N.Sugiyama, T.Mizumo, and S.Takagi, 2002 Symp. VLSI Tech. Dig. Tech. Papers, 96 (2002).

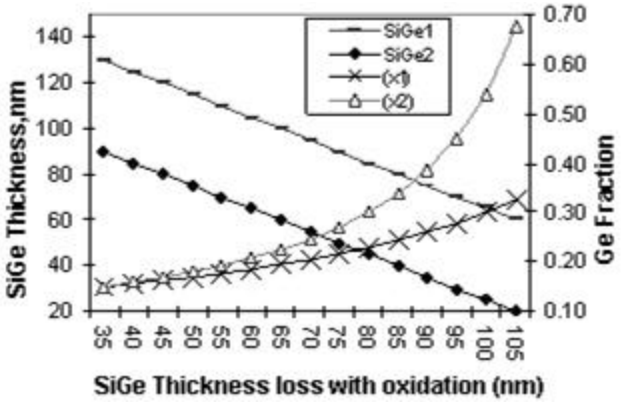

Fig. 1 : Plot showing increase in Ge concentration with decrease in SiGe thickness

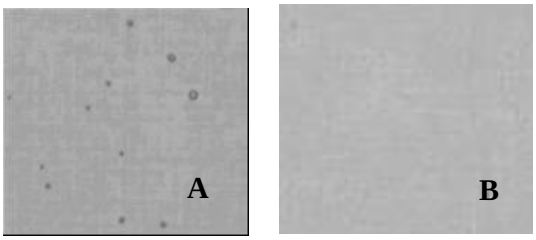

Figure 2: Optical Picture of samples without(A) and with pre-anneal(B) treatments (50X mag.)

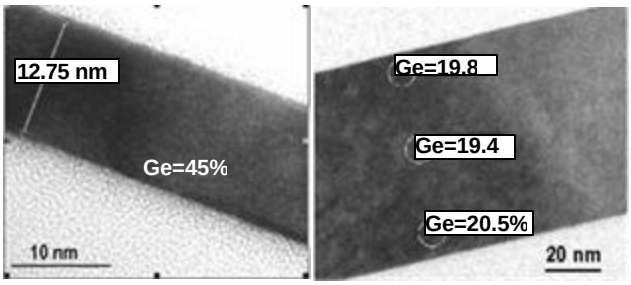

Figure 3 : Tem cross-sections of two areas on same chip showing a difference in SiGe thickness and concentration. Thicker sample is relaxed while thinner is strained.

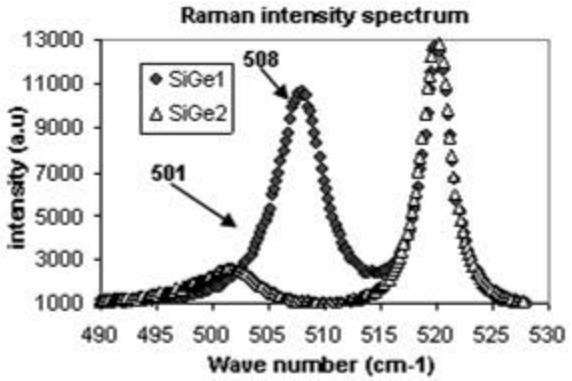

Figure 4 : Raman spectrum of two SiGe areas. SiGe1 (thicker) sample shows relaxation while SiGe2(thinner) sample shows strain.

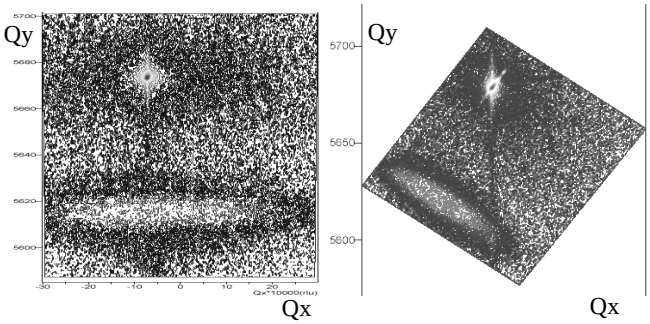

Figure 5 : XRD maps (004 and 224 directions) from. SiGe1(relaxed) sample.

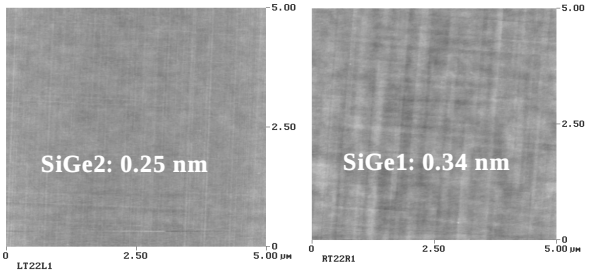

Figure 6: AFM data showing surface roughness of strained (SiGe2) and relaxed (SiGe1) samples.