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A Novel Approach to fabricate High Ge content SiGe on Insulator from Amorphous SiGe deposited on SOI wafers

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1. Introduction

In an attempt to overcome the scaling challenges of Si-based CMOSFETs, many new materials have been introduced. Among them, SGOI (SiGe–On-Insulator) has attracted intensive research interests as it provides enhanced mobility. [1] In addition, presence of a buried oxide (BOX) layer beneath the SiGe leads to a reduced junction capacitance and a lower source/drain leakage. [2] Recently, MOSFETs fabricated on such SGOI substrates with improved device performance have been demonstrated. [3] However, the fabrication of high Ge-content SGOI substrate is a challenging one. [4] Among techniques to fabricate SGOI, Ge condensation by oxidizing the epitaxially grown $Si_{1-X}Ge_X$ on SOI wafer has drawn great attention due to its simple process and easy control over Ge concentration. However, in this paper, for the first time, we report fabrication process to obtain uniform single crystalline SGOI by condensation from the co-sputtered amorphous SiGe film deposited on SOI substrates. Thus no epitaxial growth is needed. The technique is applicable for local area SiGe formation.

2. Experimental

p type SOI wafers with top Si thickness of $\sim$80 nm are used as starting substrates. 100 nm SiGe film is deposited on the wafers by co-sputtering of the pure Si and Ge targets in Argon plasma. The as-deposited samples are then oxidized in an oxidation furnace. The oxidation process is first done at a higher temperature until the Ge percentage in the film reaches $\sim$50%, and after removing the top oxide layer, further oxidation is carried out at a lower temperature below 1000 °C to ensure that the film will not melt during the whole oxidation process.

3. Results and Discussion

Fig. 1 shows the Auger depth profiling of the as-deposited sample before oxidation process. Inset shows the sample structure. The average Ge atomic concentration is $\sim$ 25%. O and C signals are also observed in the sputter deposited film. Fig. 2 shows the high resolution TEM (Transmission Electron Microscopy) image of the SGOI sample after two-step oxidation. The film thickness is found to be 43.4 nm with a uniform Ge atomic percentage of 60% as measured by EDX (Electron Dispersive X-ray Spectroscopy). In addition, TEM images also show the presence of twin defects as shown in the inset (A) of Fig. 2. The inset (B) in Fig. 2 shows the FFT (Fast Fourier Transform) image of the SGOI film which indicates that the $Si_{0.4}Ge_{0.6}$ film is single crystal nature thought dislocations and defects are observed in the film. The Raman Spectra before and after oxidation is shown in Fig. 3. For the as deposited sample, only Si-Si peak from SOI is observed as expected as the co-sputtered SiGe film is of amorphous nature. In case of the sample after oxidation, besides the intense Si-Si peak from the SOI substrate, Si-Si, Si-Ge and Ge-Ge related vibrations from the $Si_{1-X}Ge_X$ film are clearly observed. In addition, line width of the Si-Ge and Ge-Ge peaks resembles the Raman line shape of single-crystal high Ge-content SiGe films. Using the method described in Refs [7-9], we can also estimate a Ge composition > 64% in these films from the Raman peak shift where composition estimation is being carried out with reference to the unstrained phonon frequency. Such a peak shift is compensated by the amount of in-plane lattice strain. In a similar way, we can also estimate an average in-plane strain component in these layers when compared to Raman peak shift of the unstrained bulk $Si_{1-x}Ge_x$ layers. It is found that the film after two-step oxidation process possesses 0.26% compressive strain. Such an amount of strain in SGOI layers is beneficial for the improvement of hole mobility [10].

Since the amount of average in-plane strain given by Raman analysis is based on several approximations related to phonon peaks of compositional-dependent unstrained SiGe, a comparative HRXRD analysis is carried out. The symmetric ω-2θ rocking curve scan of the SGOI film after two-step oxidation is shown in Fig.4. The Ge percentage is calculated to be 61.1% which is consistent with the concentration given by EDX. The lattice constant of the SiGe (both the in-plane X and Y direction, refer to inset (A) of Fig. 4 calculated from the reciprocal space map is 5.536 Å, while the out-of-plane lattice constant of SiGe in Z direction is 5.594Å. According to Vegard's law, a fully relaxed SiGe crystal with a Ge percentage of 61.1% would have a lattice constant of 5.569 Å [11]. Hence, in X and Y directions, the SGOI film involves 0.59% compressive strain whilst in Z direction, the SGOI film involves 0.45% tensile strain. It is believed that the overall effect of these strains would improve the performance of the PMOSFET [12, 13]. The difference in the strain values estimated from Raman and XRD could be due to a difference in the probing area and depth. In addition, in literature, the phonon deformation potential constants for SiGe with Ge composition higher than 50% are not well established. Such limitations may also lead to a large fluctuation in the strain values in SGOI probed by Raman technique.

Atomic Force Microscopy images in Fig. 5 show comparable roughness of the as-deposited and after two-step oxidation. It is reported that cyclic annealing process is effective in reducing the defect and dislocation density in Ge film epitaxially grown on Si [14]. Hence, the $Si_{0.4}Ge_{0.6}$-on-insulator wafer prepared by two-step oxidation received 5 cycles of cyclic anneal between a high temperature (900℃) for 10 minutes and a low annealing temperature (760℃) for 10 minutes [14]. Fig.6 shows the TEM picture of the SGOI sample after this thermal treatment which confirms that the quality of the film is improved. In addition, no twin defects were observed after the cyclic annealing as shown in the inset (A) of Fig. 6. The inset (B) and inset (C) of Fig. 6 represent FFT image and the diffraction pattern of $Si_{0.4}Ge_{0.6}$ film respectively, which all confirm the single crystal nature of the film. In addition, as shown in Fig.7, there is no obvious Raman peak shift after the cyclic anneal which implies that the SGOI film still retains its original strain.

4. Conclusion

In conclusion, we have demonstrated a cost effective method to form high Ge content SGOI without using any epitaxial growth step. Sputtered SiGe on SOI is used to perform Ge condensation process and a cyclic annealing reduces crystal defects remarkably. It is found the strain in the $Si_{0.4}Ge_{0.6}$ is beneficial for p-MOSFETs. The

technique can be used to form local regions of high mobility layers on SOI wafers in CMOS process integration.

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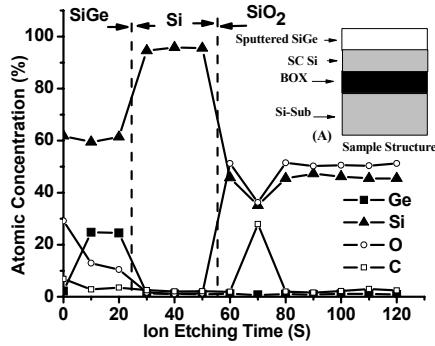[14] H.C. Luan, et al., APL, Vol. 75, p.2909, 1999.

Fig. 1 Auger depth profiling of the as-deposited sample before any oxidation process; the insert (A) illustrates the structure of the sample;
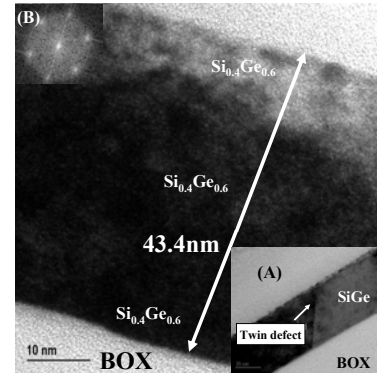

Fig. 2 High resolution TEM of the $Si_{0.4}Ge_{0.6}$ on insulator structure achieved after two-step oxidation process. Insert (A) shows the twin defect observed in the SGOI, and insert (B) represents FFT image of the SGOI film;
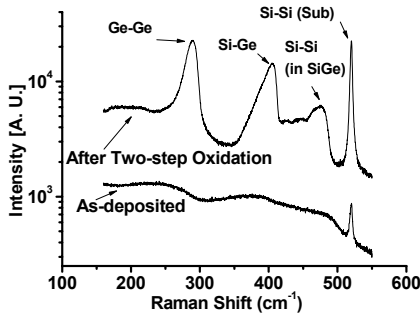

Fig. 3 Raman spectra from the as-deposited sample and the sample after two-step oxidation; Much narrower Raman modes associated with Si-Si, Si-Ge, and Ge-Ge vibration peaks reveal high crystalline quality.
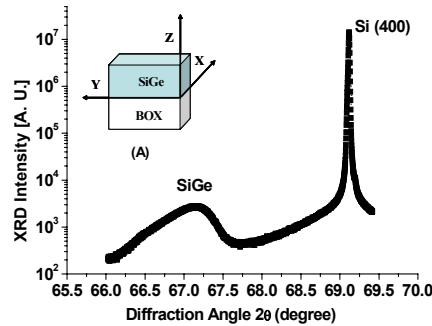

Fig. 4 XRD scans of SGOI sample after two-step oxidation process. The Si and SiGe diffraction peaks are used for Ge composition estimation.
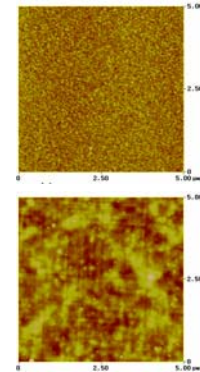

Fig. 5 AFM images of as-deposited sample (top, RMS=0.92nm) and the sample after two-step oxidation (bottom, RMS=1.05nm).
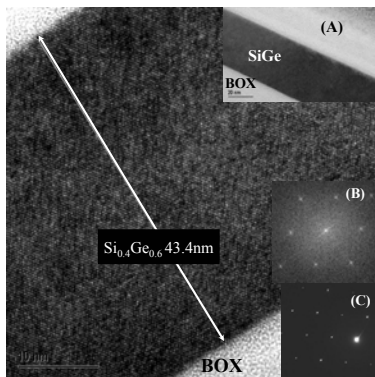

Fig. 6 High resolution TEM of the $Si_{0.4}Ge_{0.6}$ on insulator structure after cyclic thermal treatment; no twin defect is observed in the SGOI film as shown in inset (A); inset (B)
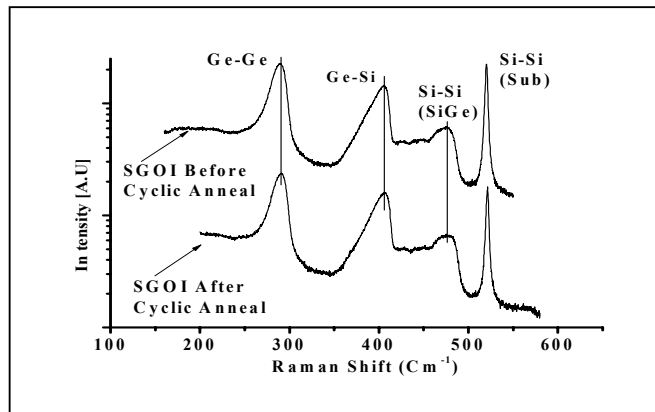

Fig. 7 Raman Analysis showing that the strain in SiGe on insulator is maintained after the cyclic annealing.