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Embedded Nanowire Network Growth and Node Device Fabrication for GaAs-Based High-Density Hexagonal BDD Quantum Circuits

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1. Introduction

Exploration of new LSI technologies beyond Si CMOS LSIs has become an inevitable issue, as the ITRS roadmap indicates in its appendix[1]. Here, the III-V nanotechnology seems to have much to offer by its capabilities of forming sophisticated nanostructures. We have recently proposed a novel hexagonal BDD quantum circuit architecture based on III-V nanowire networks [2], and demonstrated its feasibility by fabricating small-scale circuits up to a two-bit quantum adder [3] on GaAs etched nanowires prepared by electron beam lithography and wet etching. However, further reduction of wire size and pitch is required for higher density circuits operating at room temperature (RT).

The purpose of this paper is to investigate basic feasibility of high-density hexagonal BDD quantum integrated circuits utilizing MBE-based selectively grown (SG) nanowires from viewpoints of dense network formation and transport device fabrication.

2. Circuit Configuration and SG Nanowire Growth

The hexagonal BDD quantum circuit[2] is laid out on a hexagonal nanowire network such as shown in **Fig.1(a)** as a directed graph for a logic function which is called a binary decision diagram (BDD). At each node of the graph, a node device having one entry branch and two exit branches are formed, and it performs gated path switching for a single or a few electrons. Hexagonal layouts are used to take advantage of the three-fold symmetry of the node device.

Thus, the key issue is how to prepare high-density hexagonal networks. In this study, we investigated MBE-based selectively grown (SG) nanowires developed by our group [4,5]. Here, hexagonal mesa patterns corresponding
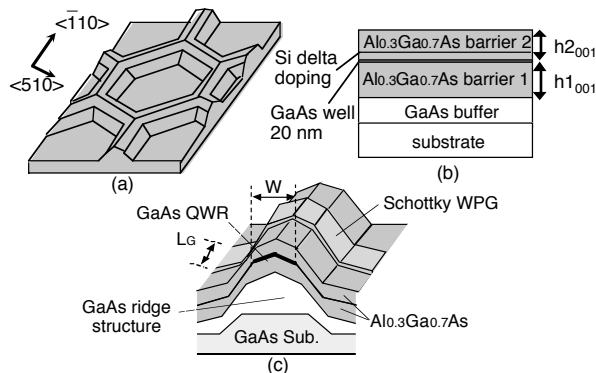
to the final wire pattern such as shown in **Fig. 1(a)** were formed on substrates by EB lithography and wet etching. For (001) substrates, $<\bar{1}10>$ and $<510>$ directions were used to form hexagons. Next, buffer ridge structures are grown by MBE. Then by growing a nominal three-layer structure shown in **Fig. 1(b)** by MBE on the buffer ridges, nanometer-sized embedded quantum wire (QWR) such as shown in **Fig. 1(c)** is selectively grown on the top of the mesa due to growth selectivity. Si delta doping was made to supply carriers. As shown in **Fig. 1(c)**, branch switches were fabricated by depositing a metal finger on the nanowire to form a wrap gate (WPG) [3].

3. Growth of SG Nanowires for Transport Devices

Cross-sectional SEM images of $<\bar{1}10>$ and $<510>$ -oriented SG QWRs grown in this study are shown in **Figs. 2(a)** and **(b)**, respectively. GaAs QWRs are clearly seen and they have different cross-sectional structures.

For fabrication of hexagonal nanowire network on GaAs, a maximum node density of 2.4×10^8 cm^{-2} has been obtained so far. **Figure 3(a)** shows an SEM micrograph. It shows smooth and uniform nature of the network. Its cathodoluminescence (CL) image is shown in **Fig. 3(b)**
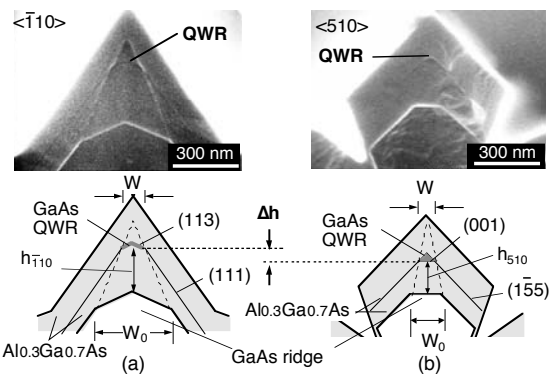

Fig. 2 Cross-sectional SEM images of (a) <-110> and (b) <510>-oriented SG QWRs.
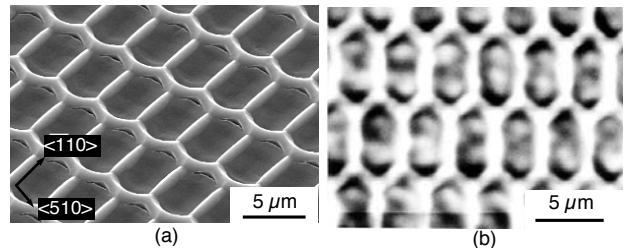
Fig. 3 (a) An SEM image of a SG hexagonal nanowire network and (b) its panchromatic CL image.

Fig. 1 (a) A part of a SG hexagonal nanowire network, (b) material supply for QWR growth and (c) GaAs SG QWR branch switch controlled by a wrap gate (WPG).

which indicated formation of optically uniform QWRs.

However, continuous CL images do not necessarily tell that wires are electrically connected. To realize electrically connected network, alignment of vertical positions of QWRs is obviously important. Therefore, the vertical growth rates of AlGaAs on $<\bar{1}10>$ and $<510>$-oriented buffer ridges were measured as summarized in **Fig. 4** as a function of the buffer ridge width, W_0. The result shows that vertical heights of QWRs, designated as $h1_{\bar{1}10}$ and $h1_{510}$ in **Fig. 1(b)**, are not the same, even if W_0 is the same. The effect of height difference, Δh, was further investigated by preparing two samples, A and B, with different values of W_0 and Δh, as shown in **Table I**. As shown in **Table I**, electrical conduction was observed even for a large value of Δh. However, the measurement clearly indicted that a small Δh value realizes better electrical transport.

Table I Sample dimensions and measured resistances

Sample	$W_0<\bar{1}10>$	$W_0<510>$	Δh	R_j (ave.)
A	600 nm	1000 nm	9 nm	7.1 kΩ/sq.
B	1000 nm	800 nm	2 nm	4.3 kΩ/sq.
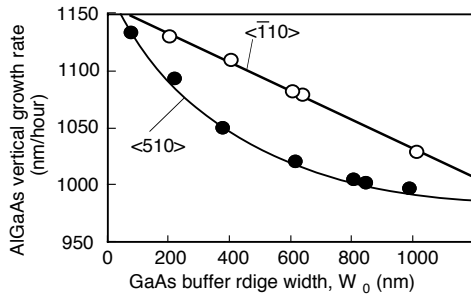
Fig. 4 Vertical growth rates of AlGaAs on $<\bar{1}10>$ and $<510>$-oriented buffer ridge structures vs. ridge width, W_0.

4. Fabrication of Transport Devices on SG Nanowires

WPG controlled branch switches shown in **Fig. 1(c)** and BDD node devices using two such branch switches were fabricated on the SG nanowires.

Figure 5(a) shows RT I_{DS}–V_{DS} curves of $<\bar{1}10>$ and $<510>$-oriented branch switches. Excellent gate control characteristics were obtained in both devices having different cross-sections. They showed clear quantized conductance at low temperatures as shown in **Fig. 5(b)**

In order further to investigate the influence of the top barrier thickness on the gate control characteristics, two kinds of $<\bar{1}10>$ and $<510>$ - oriented branch switches with two different top AlGaAs supply thicknesses, $h2_{001} = 50$ nm and $h2_{001} = 40$ nm with reference to **Fig. 1(b)**, were fabricated and compared. The resultant values of transconductance, g_m, and threshold voltage, V_{th}, both measured at RT, are summarized in **Figs. 6(a)** and **(b)**, respectively. This result confirms that thinning the top barrier is very effective in improving the gate controllability together with an expected positive shift of V_{th}. In addition, very small fluctuation of V_{th} was realized in the devices with $h2_{001} = 40$ nm.
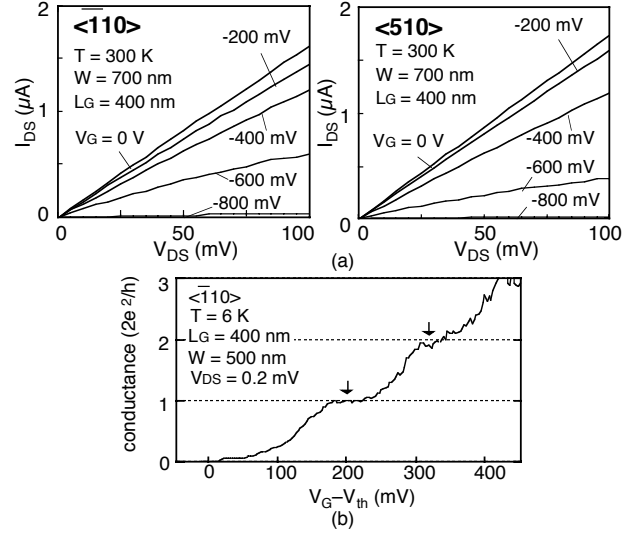
Finally, a BDD node device having two $<510>$ branch

Fig. 5 (a) Macroscopic I_{DS}-V_{DS} curves at RT and (b) conductance quantization at 6 K.
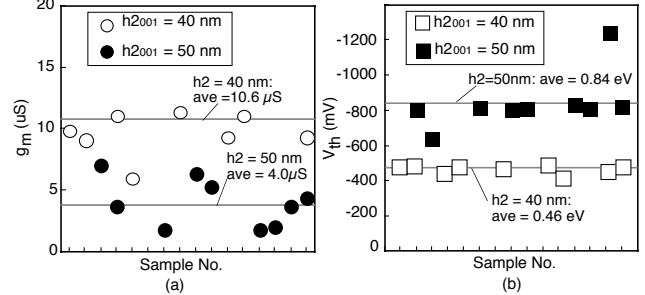

Fig. 6 (a) g_m and (b) V_{th} of devices with $h2_{001} = 40$ nm and 50 nm.

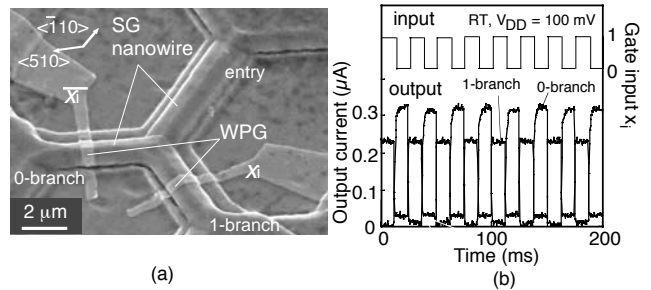**Fig. 7** (a) A SEM image and (b) path switching characteristics of a BDD node device having two $<510>$-branch switches.

switches was fabricated as shown in **Fig. 7(a)**. The device realized clear path switching characteristics as shown in **Fig. 7(b)**. This result confirms the basic feasibility of fabricating BDD devices on SG nanowires.

References

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