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GaAs DH-HEMT channel coupled InAs quantum dot memory device by selective area metal organic vapor phase epitaxy

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Devaraj Nataraj, Noboru Ooike, Junichi Motohisa and Takashi Fukui
Research Center for Integrated Quantum Electronics, Hokkaido University, North 13 West 8, Sapporo 060-8628, Japan.

1. Introduction

The quantum dots, also know as artificial atoms, has a range of potential applications. One of the key applications is in the area of single electron memory device. The quantum dot (QD) memory device mainly consists of a quantum dot layer to store electrons and a channel in close vicinity to sense the electrons in it. By applying a gate voltage the QD energy levels can be shifted with respect to the Fermi level of the channel, and depending upon their relative position, electrons can transfer either from the channel to dot or dot to channel. If QDs are charged then the channel electron concentration will be reduced resulting a low drain current, otherwise a high current will flow. The final result is a hysteresis curve.[1-3] Large number of reports are available in silicon QD memory device addressing various key features like, fabrication, room temperature operation and single electron charging effect etc.[1] However, only limited reports are available in InAs QD memory devices, and most of them involved several hundreds/thousands of QDs.[2, 3] In the present work we fabricated a InAs QD memory device with reduced number of QDs by selective area metalorganic vapor phase epitaxy (SA-MOVPE) growth method.

Since storing information in an economic way requires high packaging density and low power consumption, there is a need to reduce the number of QDs. However, if number of QDs are reduced then the size of the channel should also be reduced enough to sense a small potential change in QDs caused by the charging/discharging effects. In the present work we utilized a natural width reduction mechanism associated with SA-MOVPE to define narrow GaAs channels, and then on the top of narrow channel few InAs QDs were grown to realize a memory structure which involves few electrons for its memory operation.

2. Experiment

Narrow wire like openings with a length of 4μm along [-110] direction and a width of 600 nm in [110] direction was defined on SiO_2 masked GaAs (001) substrates by electron beam lithography and wet chemical etching methods. In this opening area, using low pressure MOVPE system working at 76 Torr, GaAs double hetero structure high electron mobility transistor (DH-HEMT) channel was grown followed by InAs QDs to complete the memory structure. The growth sequence of the channel and their thicknesses are as follows: a 250 nm GaAs buffer layer, a 50 nm $Al_{0.3}Ga_{0.7}As$ layer, a 18 nm GaAs well layer, a 10 nm $Al_{0.3}Ga_{0.7}As$ spacer layer, 25 nm Si doped $Al_{0.3}Ga_{0.7}As$ layer, and 10 nm GaAs capping layer. The growth temperature was 700°C. After the completion of the channel, growth temperature was reduced to 440°C in five minutes and then InAs QDs were grown by Stransky-Krastanow growth method. A 20 nm thick GaAs capping layer was grown at the same temperature without interruption to cover the dots, then temperature was increased to 600°C for a further growth of 50 nm thick GaAs as a second capping layer. Two similar structures were also grown, in which one sample has no QDs and the other does not have top capping layer for comparative and quantum dot analysis, respectively. The source materials used for this growth were trimethylgallium (TMG), trimethylaluminium (TMA), trimethylindium (TMI) and 20 % arsine in purified hydrogen. After the completion of growth, Ge/Au/Ni/Au metals were deposited and annealed at 450°C for five minutes for ohmic contact, and then Cr/Au metals were deposited as gate electrodes. Electron beam lithography and photo lithography techniques together with the standard lift off process were utilized to define the electrodes. The carrier density and mobility of two dimensional electron gas (2DEG) on a planner reference sample at 77 K was 1.0 x 10^{12} cm^{-2} and 53,700 cm^2/Vs, respectively. To know the number of buried QDs and its size distribution, scanning electron microscope (SEM) and atomic force microscope (AFM) analysis were done on uncapped samples, grown separately but under similar growth conditions. SEM analysis on the uncapped wire pattern has shown InAs QDs with a size distribution of 10 ~ 30 nm and with an average number of 50 dots under the gate electrode of dimension 200 x 1000 nm^2. Ex situ AFM investigations on uncapped planner samples has shown the height of QDs as ≤ 8 nm.

3. Results and discussion

Fig. 1(a) shows the cross sectional SEM image of GaAs wire grown on SiO_2 masked GaAs (001) substrates by SA-MOVPE growth method. The growth is pyramidal like with a reduced top width, because of the faceted growth behavior of GaAs on masked GaAs (001) substrates.[5] In the present work we utilized this natural width reduction mechanism to define narrow channels. For this purpose, at first we have grown thick GaAs buffer and bottom $Al_{0.3}Ga_{0.7}As$ barrier layers to reduce the top width of the wire and then grown a channel layer followed by InAs QDs to complete the memory structure. Fig. 1(b) shows the SEM image of our device structure, with reduced top width of 200 nm.

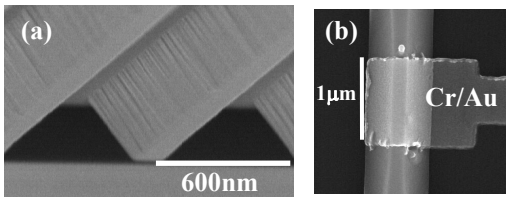

Fig. 1(a) Cross sectional image of GaAs wire (b) SEM image of device structure.

Fig. 2(a) shows the hysteresis behavior of our memory device at 20 K. The drain current was measured, in dark, for a fixed source drain voltage (V_{DS}) of 100 mV by scanning the gate voltage (V_G) from -0.4 V to 1.0 V and then in a reverse direction. The reverse scanning have resulted a positive voltage shift in the drain current showing a clockwise hysteresis with a ΔV_{th} value of 165 mV. A similar measurement from a sample without QDs has shown no hysteresis effect, and therefore the positive shift in our sample with QDs can be attributed to the electron capturing at QD energy levels. The temperature dependence on ΔV_{th} value has shown a decreasing trend from an initial ΔV_{th} value of 165 mV at 20 K to a zero value at 200 K as shown in fig. 2(b). Thermal energy assisted excitation and removal of trapped electrons is the reason for this decreasing trend. Thermal energy assisted excitation and removal of charge carriers is reported elsewhere.[6]

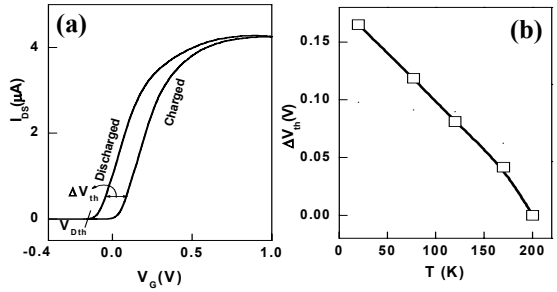

Fig. 2(a) Memory characteristics at 20 K (b) temperature dependence on ΔV_{th}

The charging/discharging process in our device can be discussed as follows. In the forward scanning, QD energy levels were lowered below the Fermi level and therefore electrons were transferred from the channel to QD energy levels, and thereby leading to a decrease in the channel carrier concentration. During the reverse scanning, because stored electrons were not released immediately, the magnitude of current flowing through the channel was less and thus resulting a clockwise hysteresis. However when the reverse scanning reached V_G = -0.4 V, the stored electrons were completely removed followed by a transferring to the channel. Fig. 3 (a, b) is the schematic conduction band profile of the channel coupled dot structure, showing the discharged and charged states.

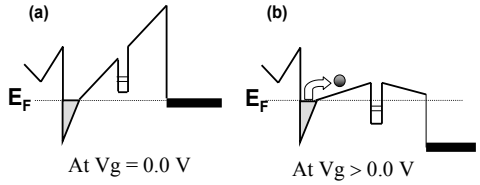

Fig. 3 (a, b) schematic conduction band profile of GaAs DH-HEMT channel coupled InAs QD memory device.

We also attempted to know the nature of charged/erased states of our device with respect to time. For this experiment, at first, we charged QDs with electrons, then measured the drain current, in real time, at a reading voltage of V_G = 0.0 V with V_{DS} = 100 mV. Fig. 4(a) shows such a real time measurements at 20 K. The curve 'a' in this figure is the measured drain current after the charging process. Fraction of stored electrons returns to the channel and gives rise to an increasing trend, because part of the occupied dot levels has higher energies than the Fermi level at the channel. The curve 'b' in this figure is the measured drain current after the discharging process. The decreasing trend was due to the loss in the channel electron concentration, followed by a transfer to QDs by tunneling process. Further from fig. 4(a) it can be seen that the write/erase states of our memory device could be discriminated for more than 5 minutes at 20 K. However, a similar measurement at 77 K has shown that the write/erase states could be differentiated to less than 100 seconds as shown in fig. 4(b). Thermal energy assisted excitation and emission across the barrier, on either direction, from dot to channel or channel to dot, respectively, after writing or erasing operation, is the reason for this behavior.

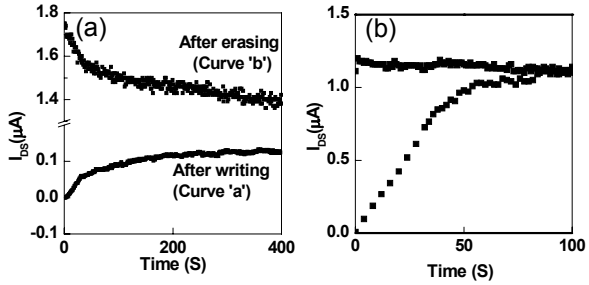

Fig.4 Real time measurements at (a) 20 and (b) 77 K.

Finally, we also calculated the ΔV_{th} of our memory device and compared the same with the experimentally obtained values. From the comparison, it was know that around 300 and 50 electrons were responsible the memory operation at 20 and 77 K, respectively.

4. Summary

In conclusion, we have successfully fabricated one dimensional GaAs channel coupled InAs quantum dot memory device by SA-MOVPE method and tested the existence of memory up to a temperature of 180 K. We utilized a natural width reduction mechanism associated with the self limited growth mechanism of SA-MOVPE to define narrow channels, and then grown few InAs QDs on the top of the channel to realize a memory device which involved few QDs, and therefore few electrons.

References:

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