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Independent Tuning of the Confinement and Density in a Quantum Point Contact using a Center Gate and a Back Gate

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1. Introduction

Transport of electrons through a narrow constriction is an elementary process underlying various phenomena in mesoscopic systems, most outstanding of which is the quantization of conductance in a quantum point contact (QPC) [1, 2] or a one-dimensional (1D) quantum wire. With present semiconductor technology, it is possible to fabricate such structures with high structural integrity, providing opportunities to explore novel physics [3, 4] profoundly distinct from what are found in macroscopic systems or systems of higher dimensions. In addition, QPCs are building blocks for more sophisticated mesoscopic devices [5], and as such their importance in connection with applications for quantum-information devices is becoming increasingly evident. In-situ and precise tuning of the properties of QPCs, therefore, is vital for both fundamental physics and device application.

Quantum point contacts are usually defined by fabricating a pair of split gates on top of a modulation-doped heterostructure and applying a negative voltage to them in order to squeeze the conduction channel underneath [1, 2]. Important structural parameters are the width (W) and length (L) of the split-gate gap and the depth of the two-dimensional electron gas (2DEG) from the surface and its initial density, which corroborate to determine the transport characteristics of the QPC [6]. The split-gate voltage, which is the only parameter tunable in-situ, modifies the confinement (and hence the energy separation between 1D subbands) and the electron density simultaneously, where the number of occupied subbands (and hence the conductance) is determined as a result of the interplay between the two.

Thus far, various approaches have been taken to add further control over the characteristics of QPCs by using a back gate [7, 8, 9] or an additional front gate separated from the split gate by etched trenches [10] or an insulator [11, 12, 13], and their usefulness in tuning the electron density has been demonstrated. In this paper, we examine a QPC device that incorporates both back gate and a center gate between the split gates to more independently control the confinement potential and the electron density. As a positive bias is applied to the center gate while applying a negative bias to the back gate to keep the same split-gate voltage at pinch-off, conductance plateaus are observed to widen, demonstrating increased confinement.

2. Experiment

The QPC device was fabricated from an AlGaAs/GaAs heterostructure grown by molecular beam epitaxy on an *n*-type GaAs (100) substrate that functions as a back gate. The heterostructure comprises a 30-nm wide GaAs quantum well modulation doped with Si at a 90-nm setback in the upper AlGaAs barrier. The quantum well is located at 260 nm from the surface, and is separated from a heavily Si-doped (10^{18} cm^{-3}) GaAs buffer layer by a 1.2-μm thick AlAs/GaAs short-period (2 nm/2 nm) superlattice barrier that prevents leakage to the back gate [14, 15]. As grown, the structure has a sheet electron density of 1.5 x 10^{11} cm^{-2} and a mobility of 3 x 10^6 cm^2/Vs at T = 1.5 K.

The wafer was processed into a square-shaped mesa (120 μm x 120 μm) with four arms on the corners, to which ohmic contacts are formed by sintering AuGeNi (80:10:10 *wt*.) at 390°C for 1 min in H_2 [15]. Standard techniques of electron beam lithography and lift-off of an evaporated 12-nm thick Ti/Au define the fine gates. All measurements were carried out at T = 1.5 K in a pumped ^{4}He cryostat using a lock-in technique with an excitation voltage of 20 μV and a frequency of 77 Hz. To avoid effects of series resistance, which varies with the gate voltages, a four-terminal configuration was employed to measure the voltage across the QPC as well as the current.

Typical results for a device with W = 0.6 μm and L = 0.4 μm are presented in Fig. 1, where we plot the measured conductance (G) as a function of split-gate voltage (V_{sg}) for different center-gate voltages (V_{cg}) ranging from –0.5 to 0.9 V. The back-gate voltage (V_{bg}) was kept at zero. The thick line corresponds to V_{cg} = 0 V. It is seen that for V_{cg} = 0 V only a small number of conductance plateaus are visible, which are not well developed at this temperature. As V_{cg} is made progressively positive, the plateaus widen, and an increasing number of plateaus become visible. For the highest V_{cg} of 0.9 V, as many as 14 conductance steps are clearly observed. On the other hand, when V_{cg} is made negative, the features become obscured until no structure (except the '0.7 anomaly' [3, 8, 9, 11]) is discernible by V_{cg} = –0.5 V. These results are consistent with previous reports [7-13], and can be understood in terms of larger subband energy separation due to more negative V_{sg} required for more positive V_{cg}.

Now we demonstrate in Fig. 2 the combined operation of the center gate and the back gate for the same device.

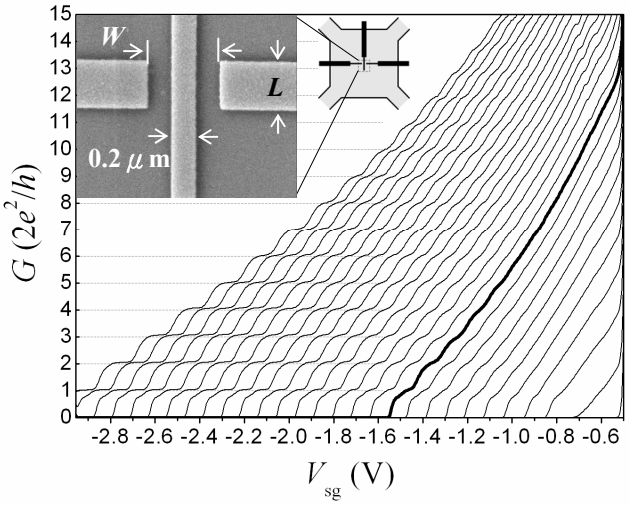

Fig. 1 Conductance (G) measured at T = 1.5 K as a function of split gate voltage (V_{sg}) for different center gate voltages (V_{cg}) from –0.5 to 0.9 V. The sample has W = 0.6 μm and L = 0.4 μm. The thick solid line corresponds to V_{cg} = 0 V. The inset shows a schematic drawing of the device structure and a scanning electron microscopic image of the fine gate structure.

Here, V_{cg} and V_{bg} are chosen to keep the same pinch-off voltage at V_{sg} = –1.76 V. The bottom trace was obtained for the condition of V_{cg} = V_{bg} = 0 V, resulting in similar structure as in Fig. 1. (The small drift in the pinch-off voltage is due to different cool downs.) As V_{cg} is increased from 0 to 0.6V while decreasing V_{bg} from 0 to –1.5V, the plateaus become wider and clearer, and a larger number of steps become visible, even for the same V_{sg}. This indicates that even though the electron density is decreased by negative V_{bg}, the confinement between two split gates are still controlled independently with center gate.

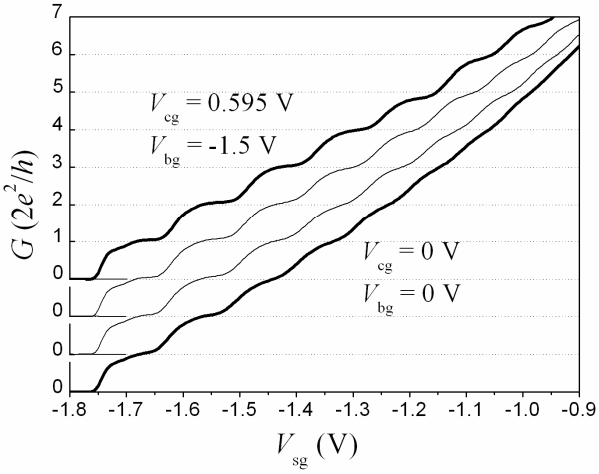

Fig. 2 Different combinations of center-gate and back-gate biases for the same pinch-off voltage at –1.76 V. The bottom trace was obtained for V_{cg} = V_{bg} = 0 V. From bottom to top, V_{cg} increases from 0 to 0.6V while V_{bg} decreases from 0 to –1.5V.

We observed, however, that these conductance plateaus were smeared out when the temperature was raised to 4.2 K. Further optimization of the device structure, including the width of the gap, the depth of the 2DEG, and its density, is necessary for operation at high temperatures [6].

3. Conclusions

We have fabricated a QPC device incorporating both back gate and a center gate. In-situ and independent control of the electron density and the confinement in the QPC has been demonstrated using the center gate in conjunction with the back gate.

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