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G-1-6

Fabrication of Fluoride Resonant Tunneling Diodes on V-grooved Si(100) Substrates

So Watanabe, Tsuyoshi Sugisaki, Yohei Toriumi, Motoki Maeda and Kazuo Tsutsui

Interdisciplinary Graduate School of Science & Engineering, Tokyo Institute of Technology
G2-26, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
Phone: +81-45-924-5461 Fax: +81-45-924-5462 E-mail: sowa@ae.titech.ac.jp

1. Introduction

Co-integration of resonant tunneling diodes (RTDs) and FETs is attractive because the higher functional circuits can be constructed with smaller number of devices compared to conventional circuits composed of only FETs. Various applications such as SRAM[1], flip-flop[2] and programmable logic element[3] have been investigated based on the compound semiconductor device technologies. However, there are few reports on the RTDs integrated with Si-based devices because high-quality heterostructures were not so easily obtained on Si substrates.

The RTD using $CdF_2/CaF_2/Si(111)$ heterostructures (fluoride RTD) is a promising candidate for a Si-based RTD. The large peak to valley current ratio (PVCR) has already been observed at room temperature[4][5], and a trial of co-integration of the fluoride RTDs and Si-MOSFETs was also reported[6]. These works indicated the high potential of this heterostructure system.

The fluoride RTDs have been usually grown on Si(111) substrates. This is because the surface energy of $CaF_2(100)$ is much larger than that of $CaF_2(111)$, so that heteroepitaxy of atomically flat CaF_2 films in (100) orientation is very difficult. However, use of (100) oriented Si substrates is highly required for co-integration of the RTDs on Si CMOS integrated circuits in future.

In this work, a new method to fabricate the fluoride RTDs on the Si(100) substrates was proposed, in which the fluoride RTDs were grown on {111} surfaces formed by using KOH anisotropic etching. The growth techniques to obtain high quality structures developed in our recent works[4, 7] were also employed. As a result, characteristics of negative differential resistance (NDR) with PVCR > 10^5 were observed on Si(100) substrates at room temperature.

2. Experiments

200-nm-thick SiO_2 was formed on n^+-Si(100) substrates by thermal oxidation. The windows in 9×9 and 9×45 μm^2 square shape were opened in the oxide layer by buffered HF etching. Then, the samples were dipped in 18 % KOH aqueous solution at 70°C for 10 min. This KOH anisotropic etching process provided V-groove structures surrounded by {111} faces in the windows as shown in Fig. 1.

Fluoride heterostructures were grown on the V-grooved substrates by MBE method, in which the two types of growth sequences, “direct-growth RTD” as shown in Fig. 2(a) or “separation-growth RTD” as shown in Fig. 2(b), were carried out. In the growth process, two techniques were employed. One is the post thermal oxidation for the first CaF_2 layer [4] in both heterostructures as shown in Figs. 2(a) and 2(b). This process is very effective to improve properties of the first CaF_2 layer by selective oxidation in pinholes generated in the CaF_2 layer. In practical process, after the first CaF_2 layer was grown on Si{111} surfaces (walls of the V-grooves), the sample was removed from the MBE system and oxidized at 500°C for 20 s in O_2 atmosphere, and then, it was loaded in the MBE system again to grow subsequent layers. The other one is introduction of the improved heterostructure as shown in Fig. 2(b) [7] rather than the conventional simple structure as shown in Fig. 2(a). In the improved structure, the layer separating the double barrier active region and the substrate interface was introduced and the alloy of $Ca_{0.3}Cd_{0.7}F_2$ was used instead of pure CdF_2. It had been demonstrated that the structure was effective to obtain high quality double barrier active region. Finally, the Al electrodes were deposited on top of both samples by using a hard mask.

I-V chracteristics of the fabricated RTDs were measured between the top electrodes and back side contact of the substrate at room temperature.

3. Results and Discussion

Figure 3 shows the top view of a 9×45 μm^2 V-groove after the KOH etching process observed by SEM. It was found that the fabrication of the V-groove structures succeeded.

Figures 4(a) and 4(b) show the *I-V* characteristics of the direct-growth RTD and the separation-growth RTD on the V-grooved Si(100) substrate respectively. As a reference, an *I-V* characteristic of the RTD on a flat Si(111) substrate, cited from Ref. [4], was shown in Fig. 5, in which growth sequence similar to that shown in Fig. 2(a) was carried out. For the direct-growth RTDs, the clear NDR characteristic as shown in Fig. 4(a) similar to those observed on the flat Si(111) substrates as shown in Fig. 5 was observed. It was shown that the new method using KOH anisotropic etching is a fine process for fabricating the fluoride RTDs on the Si(100) substrates.

However, the yield was too low for the direct-growth RTD on the V-grooved Si(100) substrate. Only 9 % devices showed NDR characteristics. On the other hand, for the separation-growth RTD on the V-grooved Si(100) substrate, 65 % devices showed NDR characteristics and most of them exhibited PVCR of 10^2 - 10^3 and the highest value was over 10^5. Thus, the good fluoride RTDs were obtained on the V-grooved Si(100) substrates by using the growth techniques represented in Fig. 2(b).

4. Conclusion

We demonstrated a capability of fabrication of fluoride RTDs on Si(100) substrates, which had been limited

only on Si(111) substrates so far. The fluroride RTDs fabricated on the V-grooved Si(100) substrates exhibited good NDR characteristics comparable to those fabricated on flat Si(111) substrates. The result indicated a promising way to realize co-integration of the fluoride RTDs and Si CMOS devices in future.

Acknowledgement

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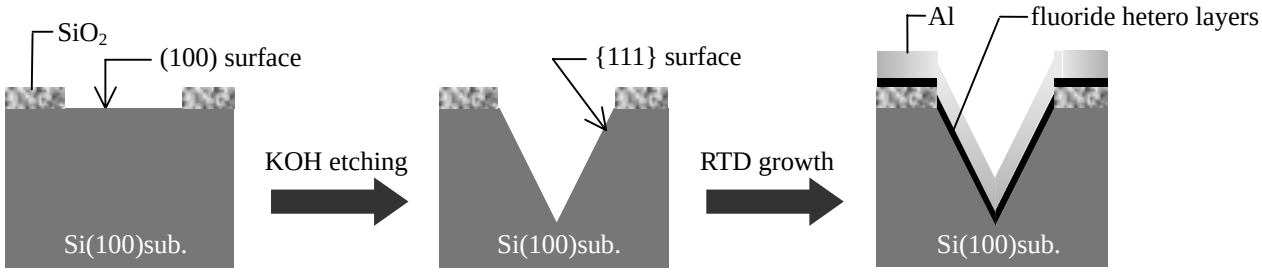

Fig. 1. Fabrication process of RTD on V-grooved Si(100) substrate.

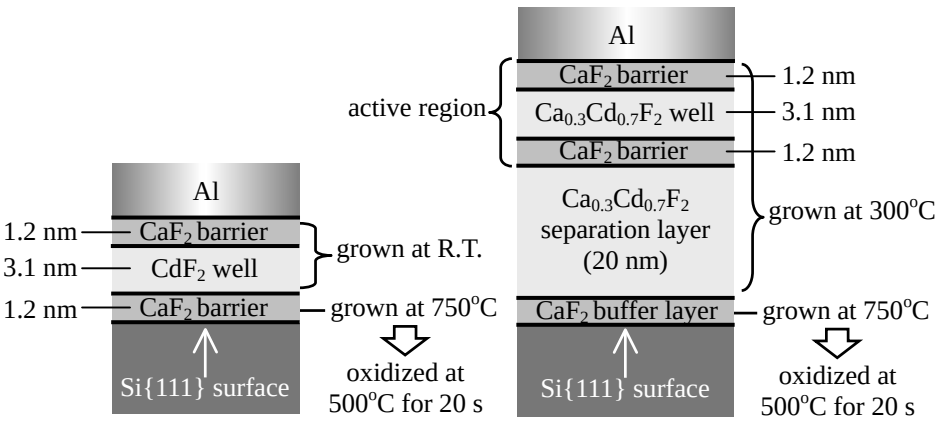

Fig. 2. Growth structures and fabrication conditions of fluoride hetero suructures. (a)Direct-growth RTD, (b)Separation-growth RTD.

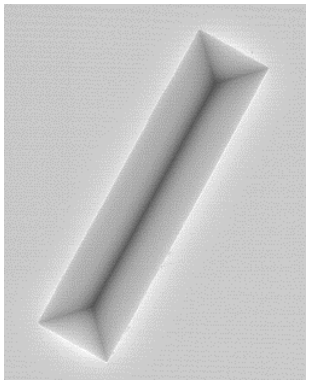

Fig. 3. Top view of 9×45 μm^2 V-groove formed by KOH etching.

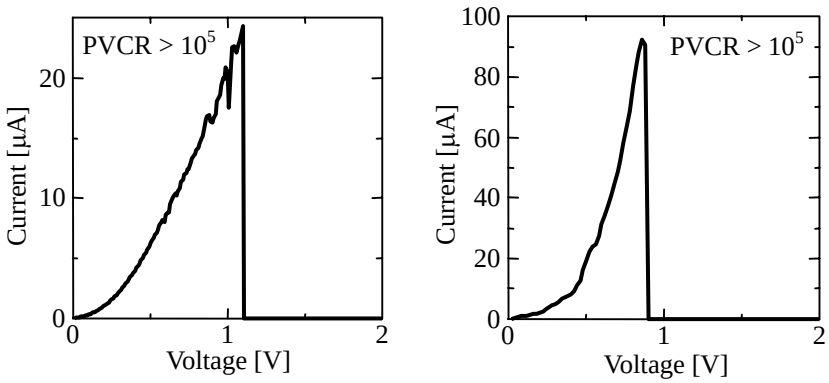

Fig. 4. *I-V* characteristics of RTDs on V-grooved Si(100) substrate (9×9 μm^2 pattern) measured at room temperature. (a)Direct-growth RTD, (b)Separation-growth RTD.

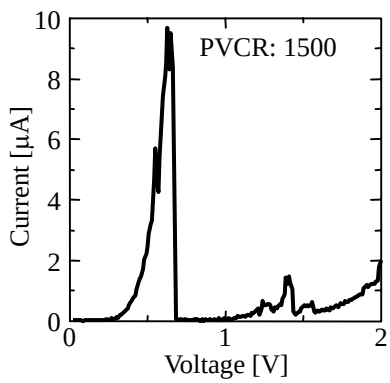

Fig. 5. *I-V* characteristic of RTD on flat Si(111) substrate (electrode: 200 μmϕ) cited from Ref. [4].