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# High Peak-to-Valley Current Ratio of $CdF_2/CaF_2$ Resonant Tunneling Diode grown on Si(100) substrates by Nanoarea Local Epitaxy

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## 1. Introduction

A $CdF_2/CaF_2$ heterostructure is an attractive candidate for quantum applications on Si substrates, such as resonant tunneling diodes (RTDs) [1] and quantum intersubband transition devices [2], because of the large conduction band discontinuity ($\Delta E_C$~2.9eV) at the heterointerface [3] and small lattice mismatch with silicon. Due to the large $\Delta E_C$, RTDs using $CdF_2/CaF_2$ heterostructures are expected to exhibit a negative differential resistance (NDR) with a high peak- to-valley current ratio (PVCR) even at room temperature (RT) [4]. Up to now, we have observed a PVCR larger than $10^5$ (at RT) for $CdF_2/CaF_2$ RTDs grown on Si(111) substrates; however, a PVCR of RTDs grown on Si(100) substrates is still small, as shown in Fig.1 [5], mainly due to leakage current. In this study, we proposed a novel crystal growth technique for $CdF_2/CaF_2$ RTDs on Si(100) substrates and observed an NDR with a high peak-to-valley current ratio of nearly $10^6$ at RT on Si(100) substrates for the first time.

## 2. Experiment

To grow high-quality $CaF_2$ thin layers on Si(100) substrates, a temperature higher than 500°C is required. However, unfortunately, the surface morphology of the $CaF_2$ thin layers formed at such a temperature is very rough, as shown in Figs.2(a) and (b), which is due to the fact that surface energy of $CaF_2$(100) is larger than that of $CaF_2$(111). To overcome this problem, $CaF_2$ was grown in small $SiO_2$ holes formed on a Si(100) substrate, which is effective for controlling the surface energy of $CaF_2$ islands grown in the holes.

A 15-nm-thick $SiO_2$ layer was formed by dry oxidation, and holes with a diameter of 80nm and a distance of 400nm were fabricated by electron-beam lithography and wet etching using HF, as shown in Fig.3.

The protective oxide layer (in the growth region) was removed in an ultrahigh-vacuum ($<10^{-7}$Pa) chamber by thermal heating with a Si flux at 700°C. Subsequently, a $CaF_2$ layer was grown at 120°C and thermally annealed at 500°C in a molecular beam epitaxy (MBE) chamber. A 1.4-nm-thick $CaF_2$ layer was formed after the annealing. A 1.6-nm-thick $CdF_2$ quantum-well layer was grown on the $CaF_2$ layer at 80°C. The top 1.4-nm-thick $CaF_2$ layer was grown on the $CdF_2$ quantum-well layer. Finally, Al/Au electrodes of 100μm$^2$ were formed by masked evaporation. The crystal growth conditions and schematic device structure are shown in Fig.4. One of the electrodes contains 40000 small RTDs.

## 3. Result and discussion

In the measurement of current-voltage (I-V) characteristics of DBRTDs, a NDR was clearly observed at RT, and the PVCR was more than $10^6$, as shown in Fig.5. The peak voltage was 1.8V. The peak current was nearly 50mA, which corresponds to 12.5kA/cm$^2$ in the growth region, and the valley current was suppressed at 15 nA. This PVCR is the highest for fluoride-based RTDs on Si(100) substrates and is as high as that on Si(111) substrates. This is because the valley current was sufficiently suppressed, and the growth areas of the Si(100) surface were covered by high-quality $CaF_2$ layers without pinholes. The peak current density was estimated to be larger than that theoretically predicted using the Esaki-Tsu formula. This is because the thickness of the $CaF_2$ barrier layers was smaller than the designed thickness by 1ML.

## 4. Conclusion

We have observed clear NDR with high PVCR for fluoride-based DBRTDs on Si(100) substrates by nanoarea local epitaxy. Crystal growth areas were limited by 15-nm-thick $SiO_2$ insulator layer and holes with a diameter of 80nm were observed. And bottom $CaF_2$ layer was post-growth annealed at 500°C. The PVCR obtained was more than $10^6$, Which is the highest for fluoride-based RTDs on Si(100) substrates.

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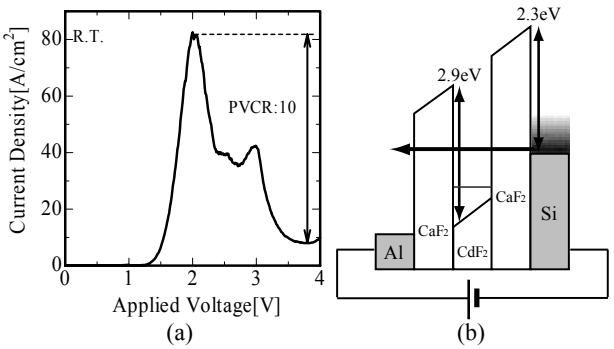


Fig.1
(a) I-V characteristic of double-barrier RTD grown by conventional technique. The maximum PVCR was nearly 10 and the current density was 80 A/cm$^2$.
(b) Band diagram of $CdF_2/CaF_2$ DBRTD.

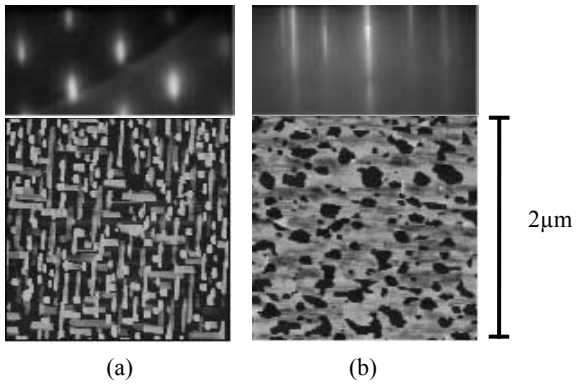


Fig.2 Surface morphology and RHEED image of $CaF_2$ samples grown on Si(100) substrates at (a) 500°C, and (b) 100°C and in-situ annealed at 500°C.

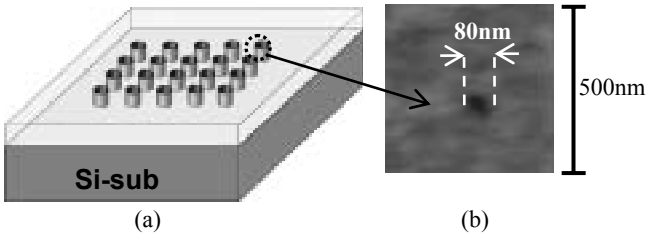


Fig.3
(a) Schematic structure of nanoarea local epitaxy substrates. Holes with a diameter of 80nm at intervals of 400nm were fabricated on a $SiO_2$ insulating layer, which was formed by dry oxidation.
(b) AFM image of growth area. The bottom of the hole is Si(100) and the surrounding area is $SiO_2$.

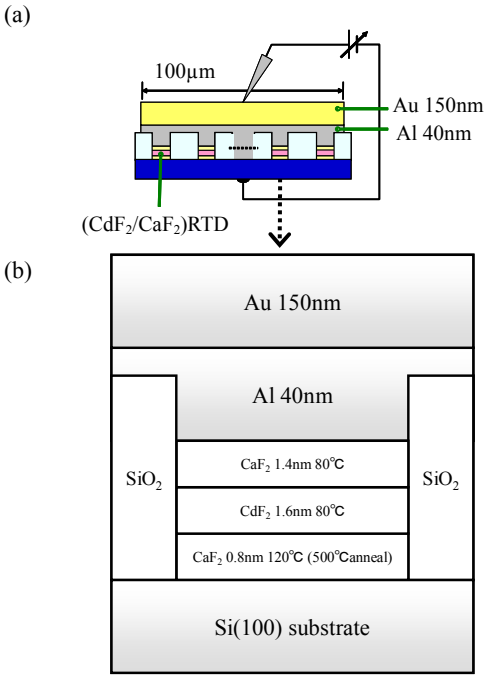


Fig.4 (a) Schematic device structure for I-V measurement. A Au/Al electrode of 100μm$^2$ was formed on the RTD array grown in sub-μm holes that were fabricated on insulator oxide. (b) Crystal growth conditions of DBRTD.

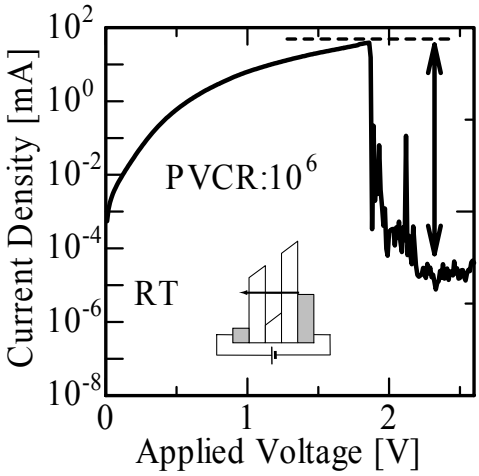


Fig.5 I-V characteristic of DBRTD at RT. The PVCR is more than $10^6$, peak current density is 12.5kA/cm$^2$ and valley current density is 4mA/cm$^2$. The effective area of the device is $5\times10^{-6}$cm$^2$.