Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.424-425

G-5-3

Temperature dependence of Space Charge Limited Current (SCLC) in thin films of silicon nanocrystals

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The temperature dependence of the conduction mechanism in thin films of silicon nanocrystals was investigated using Al/Si nanocrystal/*p*-Si/Al diodes. The device (Fig. 1) used a ~300 nm thick Si nanocrystal film, deposited by plasma decomposition of SiH_4 [1] on a *p*-Si substrate (resistivity: 10 Ωcm). The nanocrystals were 8 nm ± 1 nm in diameter and undoped, with a ~1.5 nm thick surface SiO_2 layer. Figure 1(b) shows a scanning electron micrograph of our film and Fig. 1(c) shows a transmission electron micrograph of a nanocrystal. In the later image, the oxide is ~3 nm thick, due to thermal processing before microscopy. The film is non-uniform, with ~60% nanocrystal coverage per layer, and a number density, N_{nc} ~1.2×10^{18} cm^{-3}. The film thickness of 300 nm avoids pinholes across the film. The diodes were defined using 'mesas', fabricated by electron-beam lithography and reactive ion etching. A ~150 nm-thick sputtered SiO_2 layer, wet-etched over the mesa to expose the nanocrystals, was used to support an Al top contact. The substrate-contact was also fabricated with Al. The diode area, determined by the top Al-Si nanocrystal contact area, was varied from 35 μm × 35 μm to 200 μm × 200 μm. The diode current scaled with device area. Al/Si nanocrystal/n^+-Si/Al and Au/Si nanocrystal/n^+-Si/Au devices were also fabricated and characterised.

The *I-V* characteristics of a 35 μm × 35 μm diode, measured from 300 K to 40 K using a cryogenic temperature needle prober (BCT-43MDC, Nagase & Co. Ltd.) and a Hewlett Packard 4156A parameter analyser, are shown in Fig. 2 on a log-log plot. The inset shows the room temperature *I-V* characteristics of the device from –8 V to 4 V (linear scale). Here, positive bias is applied to the substrate-contact, corresponding to a forward biased substrate. From 300 K to 200 K, the conduction mechanism is dominated by SCLC transport, in the presence of an exponential distribution of trapping states [2, 8]. Using this model, we extract a trap density $N_t = 2.3\times10^{17}$ cm^{-3} and a characteristic trap temperature T_t = 1670 K. Our value of N_t is very similar to the nanocrystal number density, N_{nc} ~1.2×10^{18} cm^{-3}. This suggests that only a few carriers are trapped per nanocrystal. In our SCLC current mechanism, holes are injected from the substrate into the nanocrystal film. These carriers can be trapped in the potential well on each nanocrystal. Single-electron or quantum confinement effects can lead to a discrete density of states in the well, limiting the number of carriers trapped in each well. This would explain our observation of similar values of N_t and N_{nc}. Alternatively, the trapping states may be formed by only a small number of defect states per nanocrystal.

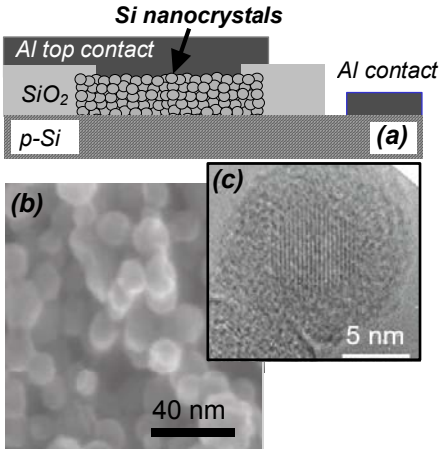

Fig. 1 (a) Schematic of the Al/Si nanocrystal/*p*-Si/Al diode. (b) Scanning electron micrograph of the Si nanocrystal film. (c). Transmission electron micrograph of a Si nanocrystal.

The values of T_t = 1670 K (corresponding to E_t = 0.14 eV) and $N_t = 2.3\times10^{17}$ cm^{-3} can be compared to amorphous Si and to other nanocrystal systems. T_t does not lie in the range observed for bulk amorphous Si (~300 K to ~1300 K) or for large (~150 nm) amorphous Si nanoparticles, and N_t is two orders of magnitude smaller than in amorphous Si [9]. Our values of T_t and N_t are more comparable to values observed in CdSe nanocrystals, similar in size to our Si nanocrystals. In CdSe, T_t ~1750 K, E_t = 0.15 eV and $N_t \sim 10^{16} - 10^{17}$$cm^{-3}$ [6, 7]. Our ratio $N_{nc} / N_t \approx 5$ is lower than in CdSe nanocrystals, where a ratio of 100 was observed for deep level traps [7]. This suggests more uniform charging in our Si nanocrystals films.

In conclusion, we investigated the conduction

mechanism in 300 nm-thick Si nanocrystal films, with ~8 nm nanocrystals. From 300 K to 200 K, we observed SCLC hole transport with an exponential distribution of trapping states, where the trap density was 2.3×10^{17} cm^{-3} and the characteristic trap temperature was 1670 K. The trap density was within an order of magnitude of the nanocrystal number density, suggesting that most nanocrystals trap single or a few carriers at most.

Acknowledgements

M. A. Rafiq would like to acknowledge the financial support from Cambridge Commonwealth Trust.

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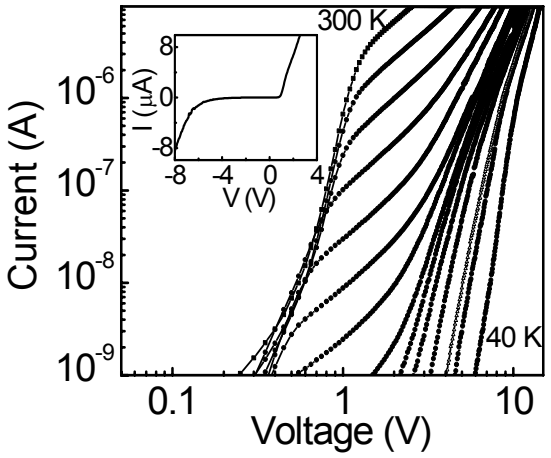

Fig. 2. *I-V* characteristics of a 35 μm × 35 μm diode from 300 K to 40 K, on a log-log plot. The temperature step is 20 K. The inset shows the *I-V* characteristics at 300 K, from –8 V to 4 V, on a linear scale.