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Topographic and Conductive AFM Measurements on Carbon Nanotube Field-Effect Transistors Fabricated by In-situ Chemical Vapor Deposition

Lorraine Rispal, Yordan Stefanov, Rudolf Heller, Gerhard Tzschöckel, Gisela Hess, Klaus Haberle, Udo Schwalke

Institute for Semiconductor Technology, Darmstadt University of Technology
Schlossgartenstrasse 8, D-64289, Germany
Phone: +49 6151 164471 Fax : +49 6151 165233 E-mail: rispal@iht.tu-darmstadt.de

1. Introduction

Since 1998, it is known that Carbon Nanotubes (CNTs) can be used in field effect transistors [1]. Single-wall nanotubes (SWNTs) can be metallic (m-SWNT) or semiconducting (s-SWNT) depending on their chirality. The s-SWNTs have a band-gap that is inversely proportional to their diameter, and act as the channel in so-called Carbon Nanotube Field Effect Transistors (CNTFETs).

In this work we have investigated the fabrication of CNTFETs growing CNTs directly on their final position between source and drain by means of a simple in-situ CVD method [2]. The macroscopic electrical characterization of the fully functional CNTFETs is complemented by nanoscale Atomic Force Microscopy (AFM) and Conductive-AFM (C-AFM) measurements on the CNTs.

2. Experimental

Si-wafers are oxidized using wet thermal oxidation (500 nm of SiO_2) for the CNTFET experiments and dry thermal oxidation (30 nm) for the C-AFM measurements. The subsequently grown CNTs are isolated by this SiO_2 from the Si-substrate which acts as a back gate electrode. Metallic source and drain regions are then structured by photolithography and lift-off. We decide to use nickel on aluminum because this combination is known to be a good catalyst for the CNT growth [3]. The thicknesses for both layers are 10 nm. Source and drain are spaced down to 1 µm and have different widths ranging from 5 to 100 µm.

The CNTs are grown on the pre-structured wafers by a two-step Atmospheric Pressure Chemical Vapor Deposition (APCVD) process. The chamber is first purged with N_2, the wafer-chuck is then heated via RF. The wafers are pre-treated during 5 min at 900°C to form nickel nanoclusters. The CNTs are then grown from this catalytic clusters in-situ at 900°C during 10 min from a methane feedstock [4]. After growth, the furnace is flushed for 1h with N_2 and without RF to cool-down the wafers to room temperature. A Scanning Electron Microscope (SEM) picture is shown in Fig. 1, indicating that first, some large diameter Multi Wall CNTs (MWNTs) have grown but stand preferably on the metal without reaching the oxide and second, thin CNTs are laying on the oxide and linking subsequently metal structures.

3. Measurements and results

First, we scan the structures with tapping-mode AFM. As a result, nanotubes with diameters between 1 and 3 nm and lengths up to 5 µm are measured on the oxide (Fig. 2). Such small diameters make us conclude that the CNTs laying on the oxide are most likely SWNTs. CNTs cannot be seen on the AFM-scan of the catalyst structures due to the roughness of the metal after heating. However, we can determine if some CNTs connect directly to the adjacent metal structures. In this case a current can be measured when a voltage is applied between the metal contacts which act as source and drain (S/D). We use a semiconductor parameter analyzer to measure the electrical characteristics of the CNT-device. For a drain-source voltage of -30V, we initially obtain an on/off ratio of about 4 (for back gate voltages of –100/100V), which indicates that both m-SWNT and s-SWNT are linking the contacts. By applying a pulse current between source and drain we manage to burn some m-SWNTs [5] and the on/off ratio improves to about 120. As a result, typical MOSFET output (Fig. 3) and sub-threshold characteristics (Fig. 4) are observed.

In order to investigate the current transport mechanism at the nanometer scale, C-AFM measurements are performed. We use the wafers with 30 nm of SiO_2 so that a direct contact between the substrate and S/D could be easily achieved providing a conducting path between AFM tip and the wafer-chuck. Current images of metal structures and CNTs are observed while the 30 nm thick SiO_2 does not allow any tunneling current for the biases we used (Fig. 5). We also performed local I-V sweeps in which the tip remains in a fixed position contacting the CNT and a bias ramp is applied. The preliminary results indicate high contact resistance and further data analysis is in progress.

4. Conclusions

By means of a simple in-situ CVD process we succeeded to fabricate fully functional PMOS-like CNTFETs with on/off ratio of 120. Since the technique is compatible with conventional CMOS processing, integrated hybrid CNT-CMOS technologies may be feasible in the future. Conductivity or work function measurements performed directly on the CNTs using Conductive Atomic Force Microscopy will provide additional information to optimize the fabrication process of CNTFETs.

References

[1] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73** (1998) 2447
[2] R. Seidel, M. Liebau, G. S. Duesburg, F. Kreupl, E. Unger, A. P. Graham and W. Hoenlein, Nano Lett. (2003), Vol. 3, No. 7
[3] R. Seidel, G. S. Duesburg, E. Unger, A. P. Graham, M. Liebau and F. Kreupl, J. Phys. Chem. B (2003)
[4] L. Delzeit, C. V. Nguyen, R. M. Stevens, J. Han and M. Meyyappan, Nanotechnologie 13 (2002) 280-284.
[5] R. Seidel, A. P. Graham, E. Unger, G. S. Duesburg, M. Liebau, W. Steinhoegl, F. Kreupl, W. Hoenlein, Nano Lett. (2004), Vol. 4, No. 5

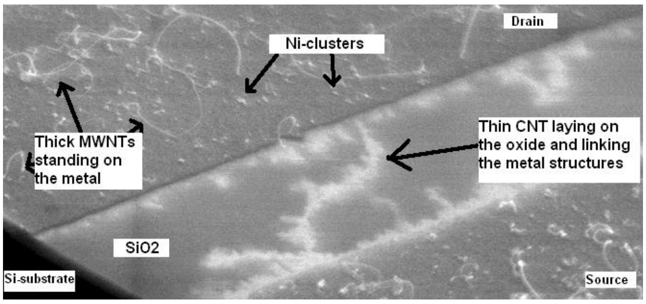

Fig. 1 SEM image of a test structure. (The wafer has been cut and tilted). The thin CNTs are visible on the oxide only because of charging effects.

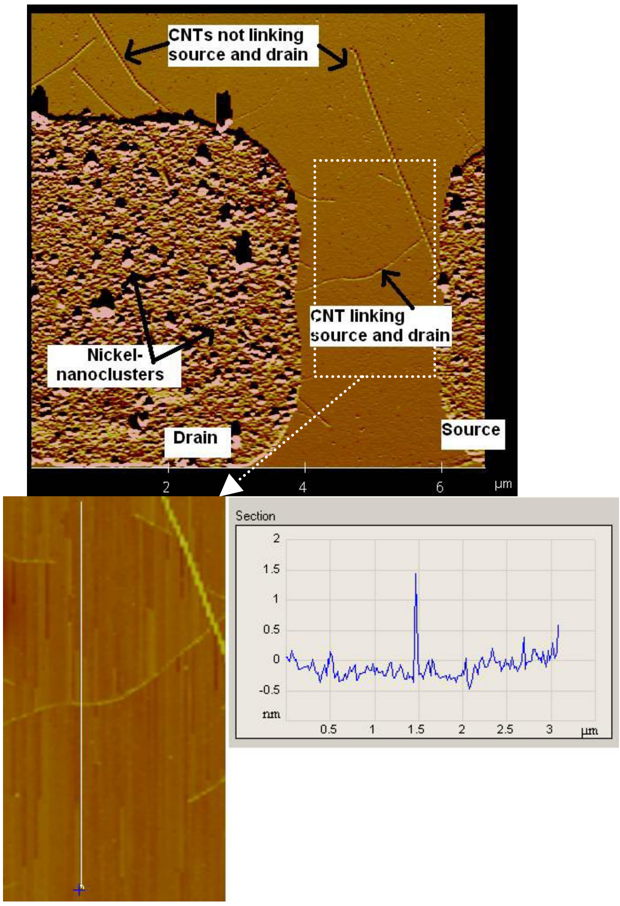

Fig. 2 AFM (tapping-mode) amplitude image of a structure (top), topography image of the linking CNT (bottom left) and cross-section along the white line (bottom right).

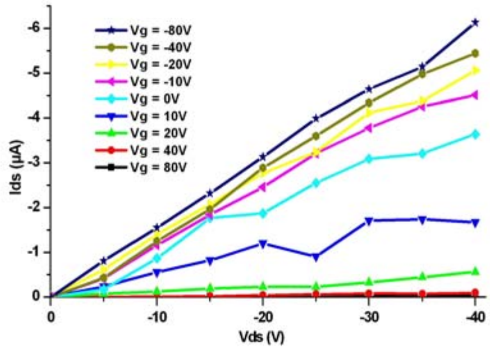

Fig. 3 Output characteristics measured on one of the fabricated PMOS-like CNTFET structures.

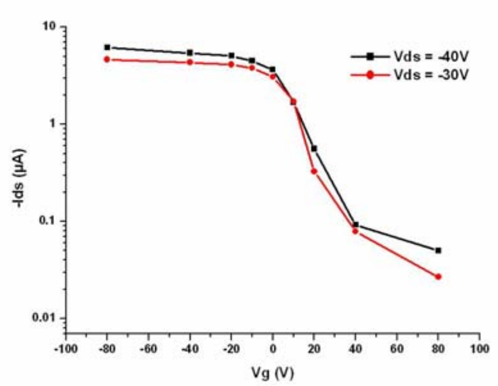

Fig. 4 Sub-threshold voltage characteristics of CNTFET (same device as fig. 3).

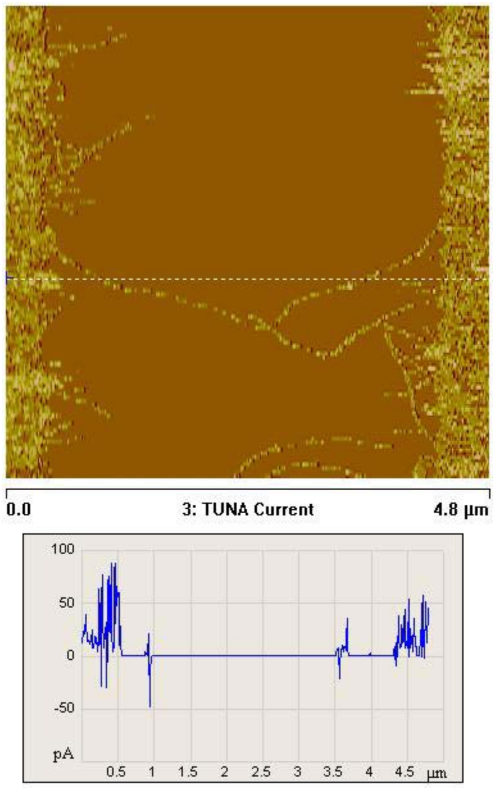

Fig. 5 Conductive AFM current image (top) and cross-section along the white line (bottom). Bias applied to the chuck: -20 mV.