Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1008-1009

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Precise Control of Island Size for Carbon Nanotube Single Electron Transistor operating at Room Temperature by AFM Electrical Manipulation

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We have succeeded in fabricating and characterizing single electron transistors (SETs) operating at room temperature with carbon nanotube channel having different island sizes. Seamless one dimensional nanoscale wire provides a basis for zero dimensional device structure by introducing small defects on it using AFM [1]. We propose a simple approach in which we cut or nick CNTs with an AFM operating in non-contact mode while scanning over the CNT.

We start with an n-type Si substrate on which we grow 400 nm thermal oxide layer. The substrate is used as a back gate. Catalyst islands consisting of Si, Mo and Fe were defined by photolithography and lift-off on the SiO_2. The CNTs with diameters of 1-4 nm were synthesized by thermal CVD using ethanol as carbon source. Metal electrodes consisting of Pt and Au were evaporated over the CNT. Figure 1 (a) shows a schematic of the experimental setup for CNT cutting or nicking. An external voltage source was used to apply a cutting voltage V_C between the CNT and the metal (Pt) coated AFM tip. Figure 1 (b) shows an example of the fabricated device before cutting or nicking. If more than one CNT connected the electrodes, we cut all undesired CNTs with AFM, leaving only one. Generally used cutting voltages ranged from -10 to -30 V. Finally, CNT SETs were fabricated by introducing two small nicks 15 ~ 30 nm apart.

The Fig. 2 shows AFM images obtained during and after applying a nicking voltage of -7.5 V. In contrast to the cutting case, nicking is not clearly noticed by AFM measurement, therefore we rely on the current-voltage measurement to verify the success of the nicking. As shown in the Fig. 3, the current level drops from 2.23 to 0.09 μA at V_{DS} = 0.3 V, which means that nicks are successfully formed. Although many devices show coulomb oscillations at room temperature we show in Fig. 4 a representative SET characteristics wich has a island length of 22 nm. The average oscillation period was 1.4 V.

In order to investigate the size dependence on the transport characteristics, we made another SET having a island length of 15 nm, which is smaller than the previous one. The oscillation characteristics of two devices are compared in the Fig. 5. The reduction in the island size is reflected as the change in the oscillation period. Three oscillation peaks are observed at voltages of -1.85, -3.2 and –5.2 V giving an average of 1.7 V for 15 nm island size SET. The oscillation period increases as expected when the size of the island decreases.

On the other hand, it is possible to estimate gate capacitance (C_G) using parameters obtained from the measurement and further compare with the geometrically calculated C_G. The values of the C_G calculated from the parameters obtained from measurement were 0.15 and 0.19 aF for 15 and 22 nm SET, respectively. These values are comparable to the C_G of 0.23 and 0.33 aF estimated from the often used analytical formula for a metallic cylinder over a plane taking into account the two different dielectric medium comprised of SiO_2 and air [2]. We have summarized the result in the Fig. 6. Since the CNTs used in this experiment are semiconducting, the discrepancy in the capacitance values can be explained by the depletion of carriers and as a result, island size reduction.

Room temperature operating CNT SETs were fabricated by introducing nicks to the CNT with an AFM operating in non-contact mode. This method is quite useful in making SETs with different island sizes and therefore control the operation characteristics like oscillation period.

[1] J. Y. Park, et. al. Appl. Phys. Lett. **80** (2002) 4446.
[2] T. Durkop, et. al. Nano lett. **4** (2004) 3539.

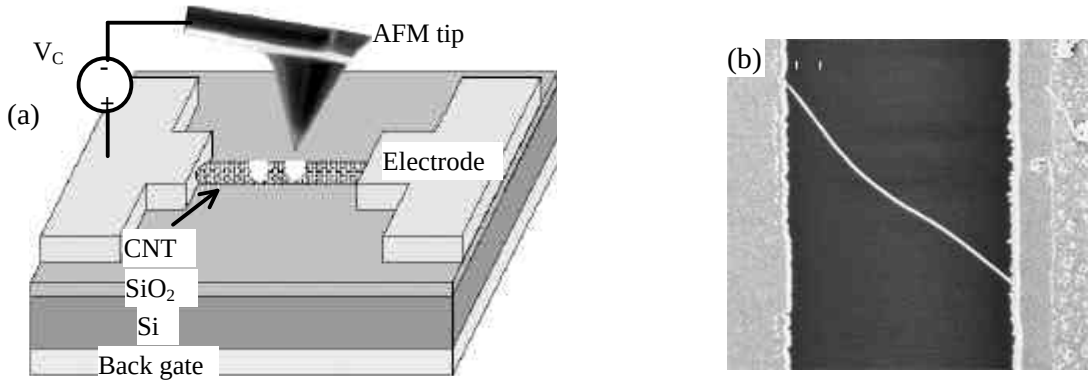

Fig. 1. (a) Schematic diagram of CNT nicking and (b) SEM image of a CNT FET

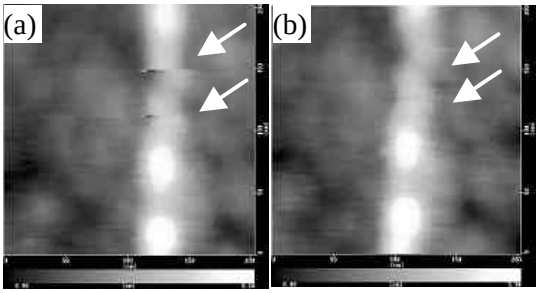

Fig. 2. 0.2× 0.2 μm^2 AFM images of (a) during and (b) after nicking with –7.5 V bias

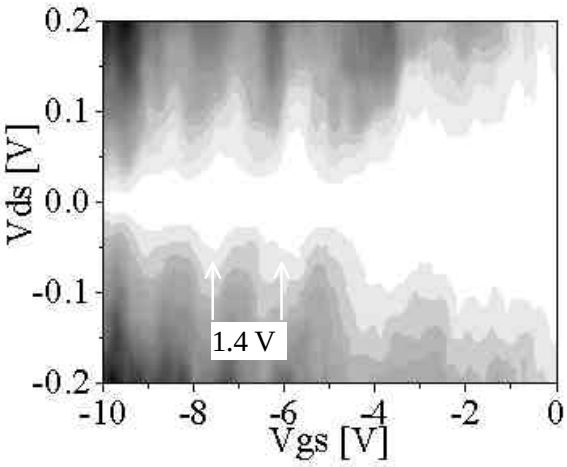

Fig. 4. Room temperature Coulomb diamonds of the device with a island length of 22 nm

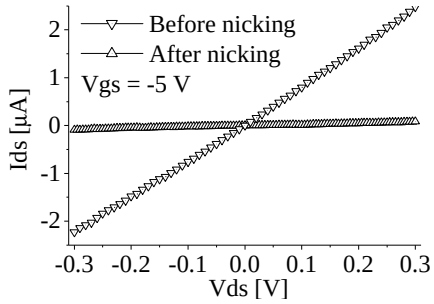

Fig. 3. I_{DS}-V_{DS} characteristics of the CNT FET measured (a) before and (b) after introducing nicks.

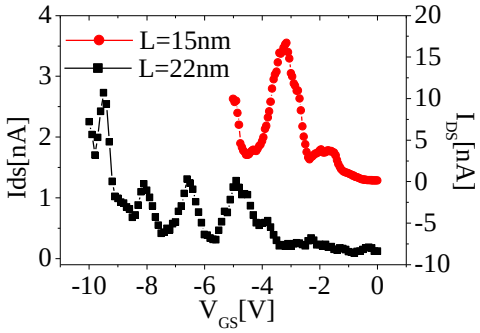

Fig. 5. Room temperature coulomb oscillation of the devices with an island length of 15 and 22 nm

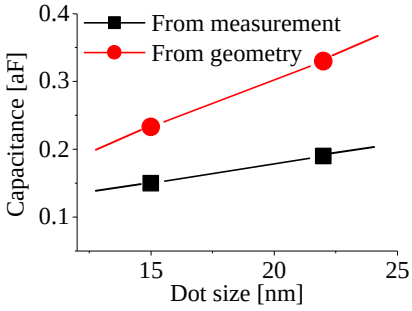

Fig. 6. Capacitance as a function of island size estimated from the measurement and geometry