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Transport and Back-Gated Field Effect Characteristics of Si Nanowires Formed by Stress-Limited Oxidation

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1. Introduction

Silicon nanowires (SiNW) have attracted attention for their application in nanoscale transistors[1-2] as well as for bio-molecular sensing.[3-5] Both top-down and bottom-up approaches have been used to realize SiNW. Top-down approaches are limited by lithography whereas bottom-up approaches are not (yet) compatible with conventional Si technology. In this work, suspended SiNW were formed on Silicon-On-Insulator (SOI) wafers using stress-limited oxidation technique. This is a top-down approach, but involves additional controlled size reduction mechanisms which allow nanowire formation in sub-10 nm scale. We also introduce a cross-sectional shape change technique. The processes are compatible with CMOS technology. Back-gated transistor configuration was used to analyze the field effect and electrical characteristics of the nanowire. Such a configuration might also be useful for binding and unbinding of the attached ionic species in the analyte for bio-sensor applications.

2. Experimental details

SOI wafers of 200 mm diameter consisting of 200 nm thick Si layer and 150 nm thick buried oxide (BOX) were used. Trenches were formed in Si up to the BOX by lithography and etching to obtain Si beams of width 80 nm. The wafers were then oxidized in dry O_2 ambient at 900ºC for 6 hrs to form nanowires at the centre of the beams. By classical oxidation model of Deal-Grove,[6] the entire silicon beam should have been consumed to form SiO_2. But due to the dynamic build-up of stress, oxidation is retarded[7] leaving a few nanometers of Si along the centre of the beam, as examined by SEM cross sections. The high resolution TEM cross section (Fig. 1(a)) shows a triangular shape of the nanowire with base 9 nm and height of 14 nm. The reason for the triangular shape is understandable from different oxidation fronts along various crystallographic orientations. By using the visco-elastic properties of SiO_2 and Si atomic migration at the SiO_2-Si interface, we can also bring about a circular shape transformation (Fig. 1(b)) by subjecting the wafers to a N_2 anneal at ~1200ºC for 1 hr. For device fabrication, the SOI was doped n-type by implantation of phosphorous (5e15cm^{-2}, 30 keV) prior to nanowire formation. The Si substrate was used as the back-gate electrode to study the field effect in the nanowire.

3. Results and discussions

The electrical transport characteristics of silicon nanowires (with a typical base and height of ~9 nm and ~14 nm respectively) were measured as depicted by the schematic test structure in Fig. 1(c). For such measurements, SiNWs were kept buried under SiO_2. The typical current-voltage (I-V) characteristics of 0.5 μm to 100 μm long SiNW are shown in Fig. 2 (a) – (b). As expected, the current through the wires increased linearly with the voltage. Also their resistance scales linearly (Fig.3) with length suggesting the uniform dimensions of the silicon wires of different lengths. The nanowires were also released (Fig. 1(d)) using dry and wet SiO_2 etching techniques and their conductance was measured. An increase in the wire resistance was observed after release, as depicted in Fig. 4 which might be related to surface passivation effects under buried condition.

The field effect transport properties of the SiNWs were studied by applying a back-gate voltage from –20 V to +20 V (figure 5) to a 100 μm long buried nanowire. Since the device works as a normally "on" n-channel FET, upon application of –ve gate bias, a depletion region is created in the nanowire channel leading to a decrease in its conductance. An increase in SiNW resistance of the order of four was observed at Vg=-20V (Fig. 6). The device does operate in the enhancement-mode with positive gate bias but a less significant increase in the wire conductance was observed (Fig. 5). This can attributed to high doping used. In the back-gated configuration, the gate dielectric thickness is quite large (estimated to be 177 nm). This would lead to reduced gate control. In addition, the substrate Si is only nominally doped and hence its depletion layer at the interface with BOX-SiO_2 layer will also contribute to the gate capacitance and reduced gate control. Thus the need for large gate voltages to observe transfer characteristics as shown here is reasonable. For shorter length nanowires, the gate control is further reduced by mechanisms similar to the classical short channel effects in MOSFETs. The Id-Vg of the back-gated transistor of wire length 100 μm is shown in Fig.7. The on/ off current ratio is ~ 10^4 and the sub-threshold slope is 770 mV/ decade.

For sensor applications, back-gated configuration might be useful for binding and unbinding of the attached ionic species in the analyte under study.

4. Conclusions

We have successfully fabricated n-type silicon nanowires (~10 nm thick) using standard CMOS compatible technology. The cross-section of the nanowires is typi-

cally triangular which can be converted to circular using high temperature annealing. The nanowires formed in this manner can be used for bio-molecular sensing applications. As the process is CMOS compatible, it can also be possibly integrated with signal conditioning circuits for such sensors.

References

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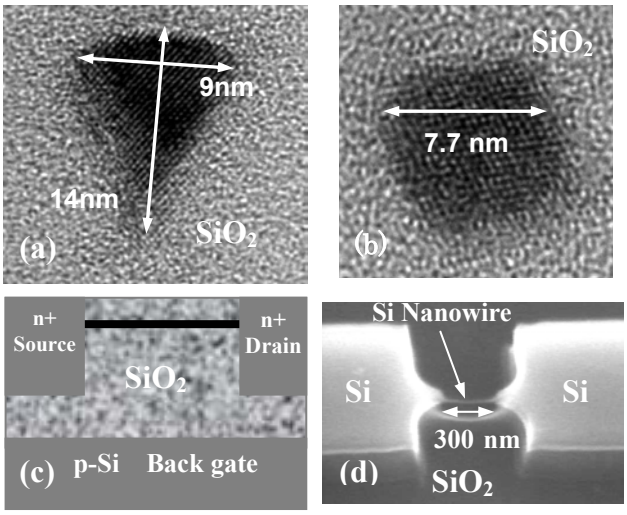

Fig. 1 (a, b): HRTEM image of cross section of the nanowires before and after annealing. (c) Schematic test structure of the SiNW device. (d) SEM image of released silicon nanowire.

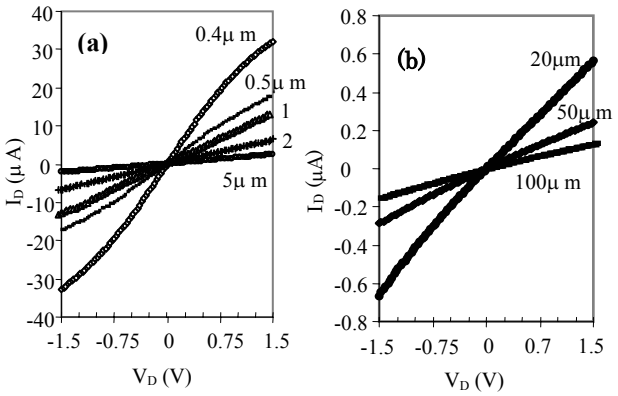

Fig. 2: I_D-V_D characteristics of Si nanowires buried in SiO_2 (a) 0.4μm to 5μm long (b) 20μm to 100μm long.

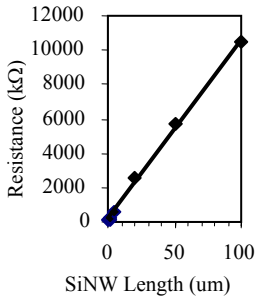

Fig. 3: Resistance scaling linearly with the length the silicon nanowires.

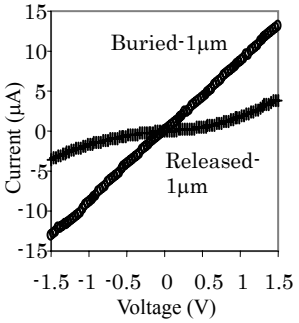

Fig. 4: I_D-V_D characteristics of 1μm long Si nanowires buried in SiO_2 and released.

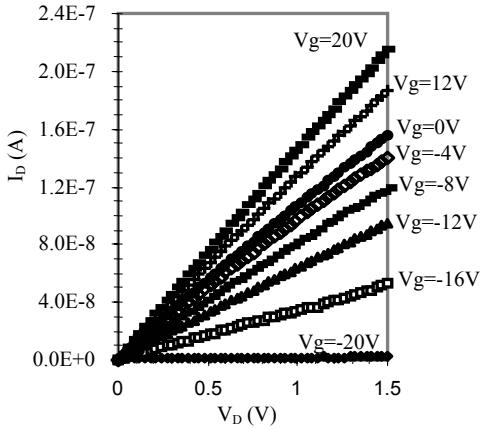

Fig. 5: I_D-V_D of 100μm long SiNW at Vg = -20V to 20V.

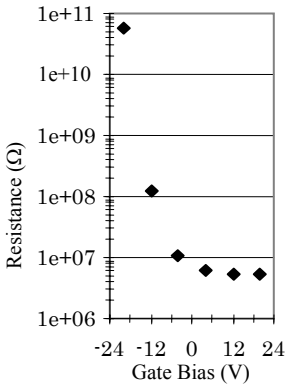

Fig. 6: Resistance modulation of 100μm long SiNW by Gate bias.

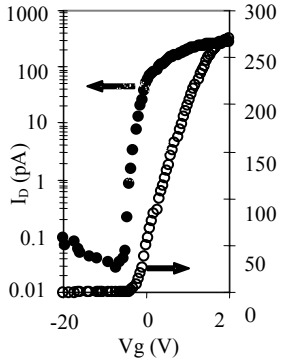

Fig. 7: I_D-V_g of 100μm long SiNW at V_D = 1.5V