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Physical and Microscopic Understanding of Data Retention Properties of DRAM

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1. Introduction

Low power consumption devices are required because portable electronic equipment is being increasingly used through the world. DRAM also requires low power consumption. However, data retention properties need to be improved to achieve this because DRAM requires a long refresh cycle. In general, the data retention times among all cell transistors in a DRAM chip are plotted as cumulative failed bit rates versus logarithmic data retention times (Fig. 1). If the distribution is compared for various process conditions, the optimal process can easily be found. In this paper, using some past experimental results, we compare how the distribution changes under various process conditions. The elucidation of the generating mechanism of process-induced defects is shown to be important to control this distribution. We herein introduce the microscopic structural analysis of the defects that we found in tail bits, as well as the physical generation mechanism. The high validity of physical and microscopic analysis that we found is described along with an improvement in the data retention property.

2. Change in data retention time distribution under various process conditions

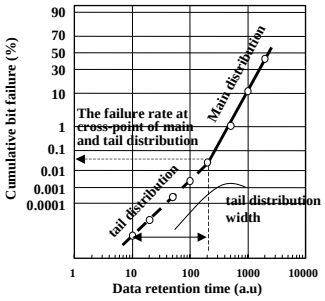

Fig. 1 Typical distribution of data retention time. The distribution can be divided into two parts, main and tail distribution. The failure rate at the cross-point of main and tail distributions corresponds to the number of tail bit.

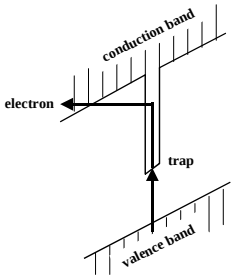

Fig. 2 Energy-band diagram of a depletion layer around a trap in reverse-biased junction. Leakage current flows through a trap in energy-band gap. Tunneling-enhanced emission of a electron from a trap (trap-assisted tunneling) is indicated. The Trap-Assisted Tunneling (TAT) current depends on the electric field strength around a trap.

As shown in Fig. 1, the data retention time distribution can be divided into two parts, main and tail. Each of these two distributions changes separately depending on the process conditions. Data retention time is determined by the junction leakage current. Also, the data retention time is dependent on both an electric field and defects because the junction leakage current flows through the carrier-trap in depletion region shown in Fig. 2 [1,2,3]. If defects are in the depletion region, the leakage current through trap-assisted tunneling process will increase in the strong electric field. Therefore, the type of the defects and the electric field strength around them become important. We need to reduce the boron concentration to improve the tail distribution because the electric field increases with a channel doping concentration.

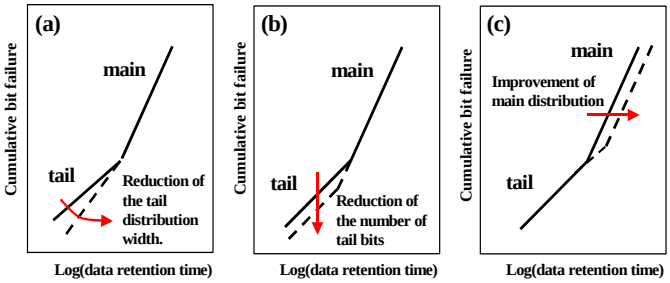

Fig. 3 Three movements of distribution lines in the cases of (a) reduction of the tail distribution width, (b) reduction of the number of tail bits and (c) improvement of main distribution.

First, we introduce the experimental examples that directly reduce the boron concentration and the example for which the boron concentration decreases by oxidation enhanced diffusion (OED). The tail distribution width is narrow because it reduces the implanted dosage of boron [4,5]. The tail distribution changes as shown in Fig. 3(a). Moreover, oxidation is performed after gate electrode etching to recover the oxide leakage current at the gate edge. The concentration of boron decreases as the oxidation thickness increases because the OED enhances the boron diffusion. The increase in recovery oxide thickness narrows the tail distribution width [4]. Asymmetric source and drain junction profiles [6] and a negative-voltage word line technique [7] were proposed as methods for lowering the electric field.

Second, we describe the effect of grown-in defects or etching damage on the number of tail bits. As shown in Fig. 3(b), the failure rate at the cross-point of the main and tail distributions decreases as oxide precipitate is decreased [8]. The report indicates that the number of tail bits increases with oxide precipitate because the number of tail bits corresponds to failure rate at the cross-point of the main and tail distributions. In addition, the number of tail bits decreases by changing the over-etching conditions using the continuous wave bias method instead of the time modulation bias method [9]. However, it dose not indicated the nature of the defect, which cause tail bits. We need to investigate how the etching damage influences data retention degradation in order to improve data retention property.

Third, the main distribution was reported to improve by using hydrogen annealing [10]. A hydrogen atom is known to combine with a silicon-dangling bond of a Si/SiO2 interface. The data retention time of the main distribution increases as a terminated bond is increased, as shown in Fig. 3(c). Furthermore, a long data retention time for a main distribution can also be observed for a shallower STI [11]. The STI depth decreases as the strain value in the

active region decreases [12]. Because a strained Si/SiO2 interface introduces a silicon-dangling bond, the dangling bond density at the interface of the STI sidewall or the gate oxide is thought to change for each stress condition.

The following are some examples that simultaneously change in both main and tail distributions. Studies have found that the improvement in the main distribution and the reduction in the number of tail bits simultaneously occur due to lower STI stress [11,13]. However, these studies were unable to clarify the origins that improved the main and tail distributions.

In addition, both the data retention time of the main distribution and the number of tail bits improves due to post cleaning after polycide gate etching [14]. Metal impurity at the Si/SiO2 interface increases trap density, and metal precipitate into the substrate causes local enhancement of the electric field [15]. Because post cleaning can remove damaged oxide, unwanted byproduct and metal contaminant, we believe that a reductions in metal at the interface and its precipitate into the substrate cause an improvement in the main distribution and a reduction in the number of tail bits, respectively. However, existence of metal precipitate or the other defect is not indicated.

The origin of the tail distribution has not yet been clarified as summarized in table 1, even though it is a very important subject. Therefore, we investigated the origin using physical and electrical analysis [16].

Table 1 Possible degradation origins for each three degradation types

Degradation types	The process conditions	Possible degradation origins
Reduction of the tail distribution width.	- Implanted boron dosage in channel region [4,5,6]	- Electric field strength
	- Recovery oxidation thickness after gate etching [4]	- Electric field strength ?
Reduction of the number of tail bits	- Gate etching condition [9]	- Etching damage ?
	- Post cleaning after gate etching [14]	- Metal precipitate ?
	- Annealing condition after STI formation [11,13]	- Stress-induced defect ?
	- Position dependence in a silicon wafer [8]	- Oxide precipitate
	- The crystal growth conditions under wafer production [13]	- Grown-in defect, process-induced defect or IG effect ?
Improvement of main distribution	- Hydrogen termination [10]	- Dangling bond at Si/SiO2 interface
	- STI depth [11]	- Dangling bond at Si/SiO2 interface or stress-induced defect ?
	- Post cleaning after WSi gate etching [14]	- Metal at Si/SiO2 interface ?
	- Annealing condition after STI formation [11,13]	- Dangling bond at Si/SiO2 interface or Stress-induced defect ?
	- The crystal growth conditions under wafer production [13]	- Grown-in defect, process-induced defect or IG effect ?

3. Process-induced defects that degrade data retention time of tail distribution

First of all, the tail bits in the tail distribution were directly analyzed by various TEM techniques. Triangular defects, which could be identified as the intrinsic stacking faults (vacancy-type stacking faults), were observed near the gate electrode edge [16]. The nature of the defect was determined by rocking curve measurement by Convergent-Beam Electron Diffraction (CBED) and TEM contrast technique. However, we found, from the result of electrically detected magnetic resonance measurement (EDMR), that small vacancy clusters cause leakage current through the p-n junction [17]. A spin-dependent carrier trap can be detected by monitoring a change in trap assisted tunneling current through magnetic resonance by the EDMR method. The triangular defect was thought to grow due to a combination of stress and silicon vacancy because the origin of the vacancy cluster can be attributed to the combination of residual vacancy induced by ion implantation and the compressive lattice strain. Strain profile in a cell transistor was measured by the CBED technique [18]. Based on the results of the defect nature and the strain measurement, we proposed a stress-related model of the triangular defect growth. According to our model, because the origin of the triangular defect can be attributed to a combination of residual vacancy induced by ion implantation and a compressive lattice strain generated by STI and gate mechanical stress, the internal stress in the gate and STI materials can be carefully controlled to relax the lattice strain. As a result, the data retention time of the DRAM product is drastically improved. By using detailed physical analysis, we clarified the cause of the tail bit and efficiently improved the data retention time.

Finally, judging from many past reports, mainly the relationship between various process conditions and data retention time has been the focus of investigations. Therefore, the information on the characteristics of the degradation origin using the indicators for controlling a tail distribution must be insufficient. In the future, device size reductions will increase the occurrence of various process-induced defects, such as stress-induced defects. Therefore, the DRAM manufacturing process will need to be optimized based on the analysis results of a process-induced defect.

4. Conclusions

We performed physical and microscopic analysis to clarify the generation mechanism of process-induced defects. Device size reductions will increase the occurrence of various process-induced defects, such as stress-induced defects. Consequently, preventing process-induced defects by using detailed advanced analysis will become necessary to improve data retention time.

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