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Optimization of Layout and Doping Profile Design for BT(Body Tied)-FinFET DRAM

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Abstract

In this paper, a device design guideline of sub 60nm BT-FinFET (Body Tied Fin FET) DRAM cell transistor is proposed. The V_T controllability and variation were compared for 3 different implant concepts (blanket, local channel, and asymmetric S/D) and 2 different fin active designs (uneven and straight active type). Those were systemically analyzed for sub 60nm BT-FinFET device. And finally, the optimal structure for mass production is discussed.

Introduction

Body tied FinFET cell DRAM has been intensively investigated [1-2] to introduce this technology to mass production early as possible. And NWL (Negative Word Line) and damascene technology were successfully applied to 512M FinFET DRAM. Based on the damascene FinFET DRAM process, LCI (Local Channel Implantation) on FinFET was shown excellent data retention time owing to reducing unnecessary boron dopant at the n+ storage node and n- region. And <100> channel direction scheme was also introduced to increase the saturation current and speed by maximize the electron mobility. However, the boron dopant at the LCI region diffuses to the storage node resulting in unwanted junction leakage increment. And the saucer type uneven active was not effective for using <100> CW (Channel direction Wafer) [4] because it has a concaved channel direction. Therefore, we have investigated a design of active fin and channel V_T control methods.

In this paper, we present several critical points of device design consideration of body tied FinFET DRAM such as the active fin design, NWL, refresh characteristics and FinFET V_T control.

Experimental

The highly manufacturable 512M damascene BT-FinFET DRAM was integrated on p-type bulk Si (100) wafer by using 80nm body tied finFET process technology [2] (Fig. 1-(a)). And LCI (Local Channel Implantation), Blanket and ASD (Asymmetric Source Drain) implantation methods (Fig. 1-(b)) were split on d-FinFET (damascene FinFET) DRAM having 2 different active designs (Fig. 2). As can be seen clearly, straight active designed FinFET shows uniform fin width of 60nm from storage node edge "A" to bit line node edge "B" while uneven active FinFET shows thicker fin width at "B" side. The refresh characteristics of FinFET DRAM were evaluated for negative word line potential versus FinFET threshold voltage and 3 different implantation schemes.

Results and Discussion

The dynamic and static refresh characteristics of 512M d-FinFET were evaluated to find a relationship between NWL and V_{TC} (Threshold voltage of Cell Tr.) of FinFET (Fig. 3). It is shown that approximately -0.6 ~ -0.8V range of NWL potential was required to minimize both dynamic and static fail bit for a FinFET cell Tr. having low (~0.1V) cell threshold voltage. And the range can be increased when higher V_{TC} was used because the dynamic refresh fail was suppressed at lower NWL where the increasing of static fail bit is still negligible. Therefore, the minimum V_{TC} was found to accomplish the operational refresh margin. However, the threshold voltage adjustment is more difficult for thinner body FinFET due to segregation of boron at the 3D fin surface. And it is ultimately difficult for DRAM because storage node junction leakage current is very sensitive to increasing of boron dopant. ASD (Asymmetric Source Drain) implantation scheme was then applied to minimize the boron effects on storage node junction leakage. Fig. 4 shows ASD device having the lowest storage node junction leakage current over the blanket implant and LCI scheme. However, the bit line node leakage current difference was minimized which has negligible effect on refresh characteristics. In Fig. 6, the threshold voltage controllability of uneven and straight type active design. ASD implantation was used and found that the V_T control of uneven active FinFET can be easier than that of straight active. It was important result because the uneven active has been conventionally used to achieve enough alignment margins after gate pattering for bit line contact. Fig. 7 shows Id-Vg characteristics of ASD implanted FinFET DRAM cell. It indicates one cell transistor can have two different V_T for operation conditions and V_T of write "1" condition is about 350mV lower than read "1" condition. It is a great advantage that the data "1" can be easily written for ASD FinFET.

However, the threshold voltage distributions of both active designs indicate a demerit of uneven active FinFET cell transistor (Fig. 8). Also V_T distribution of 80nm RCAT (Recess Channel Array Transistor) [3], FinFET with ASD and thin body transistor with TiN gate were compared. The uneven active FinFET with ASD shows large V_T distribution while recess channel array transistor and straight active FinFET with ASD show negligible distribution. It is quit clear that RCAT or straight active design is acceptable for mass production. However, FinFET cell array transistor has several advantages over RCAT besides V_T distribution for being used sub 60nm regime [1]. Therefore, based on these result, the optimal design scheme of FinFET DRAM is straight active combined with ASD or workfunction optimized gate since NWL (Negative Word Line) scheme was found to be an optimal solution for body tied FinFET DRAM.

Finally, the refresh characteristics of 3 different V_T adjustment implant scheme were evaluated (Fig. 10) and found the ASD implanted 512M FinFET DRAM shows superior characteristics over the others. Fig. 11 shows the expected V_T of sub 40nm FinFET cell DRAM by using 4.7 ~ 5.1eV gate material and minimum required V_T can be lowered for FinFET with NWL and high workfunction gate material while maintaining minimum Ion/Ioff ratio requirement of 10^9.

Conclusion

In this paper, we systemically analyze 80nm body tied FinFET cell array transistor DRAM for the fin active design and device design schemes. Based on consideration of V_T controllability, distribution and refresh margin, straight active design with ASD (Asymmetric Source Drain) scheme was found to be the best structure for production of BT-FinFET DRAM.

References

[1] C. H. Lee, et al., VLSI 2004, 13.3, p130.
[2] C. Lee, et al., IEDM 2004, 3.2, p61.
[3] H. S. Kim, et al., IEDM 2003, 17.2, p411.
[4] T. Komoda, et al., IEDM2004, 9.3, p217.

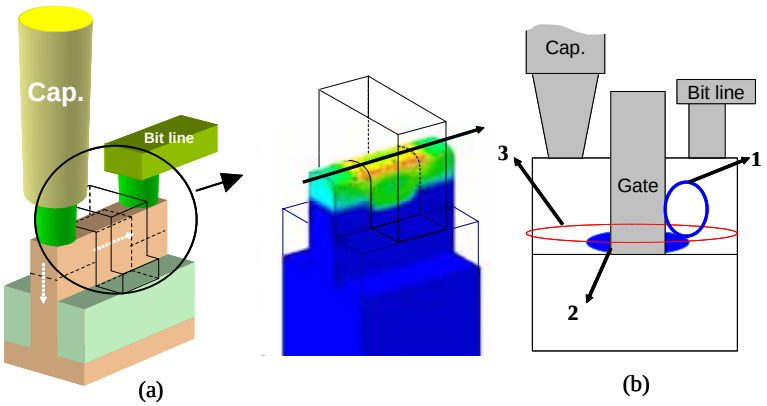

Fig. 1. Body tied FinFET DRAM device design scheme 1.Asymmetric S/D implantation 2. Local channel 3. Blanket V_T adjustment implantation.

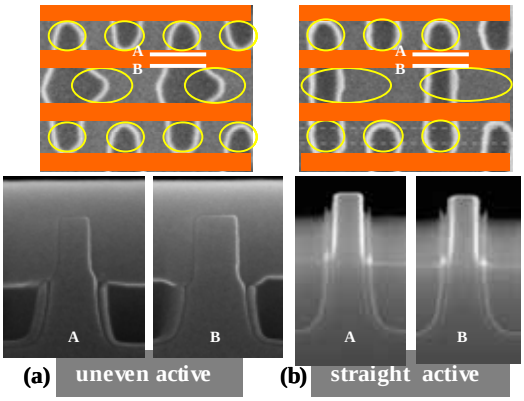

Fig. 2. Top view and vertical view SEM image of (a) uneven (b) straight active body tied FinFET cell transistor.

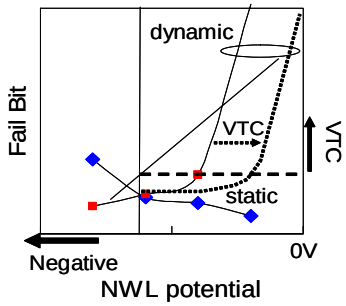

Fig. 3. NWL (Negative Word Line) potential versus Refresh results of FinFET DRAM. At the certain NWL level, static fail bits start to increase due to GIDL. The optimal V_{TC} level is required to maximize the refresh time.

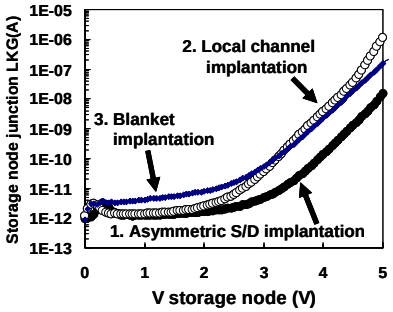

Fig. 4. Storage node leakage current characteristics. Blanket and local channel implantation device shows 1 order higher leakage current than that of ASD (Asymmetric S/D) implanted device. It is critical for refresh characteristics.

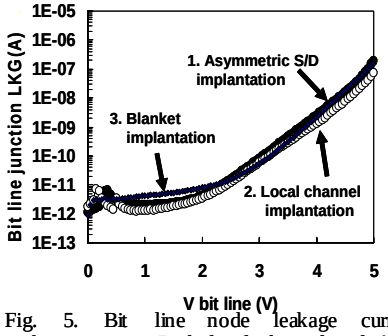

Fig. 5. Bit line node leakage current characteristics. Both local channel and ASD (Asymmetric S/D) implanted devices show almost same leakage current while blanket implanted device shows higher leakage at lower Vg.

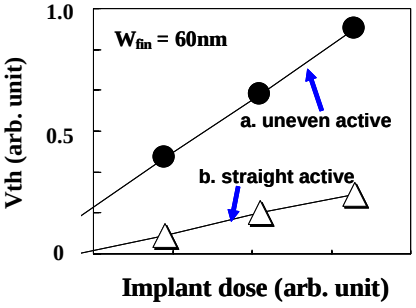

Fig. 6. V_T controllability of uneven and straight active finFET cell transistors. Asymmetric S/D implantation was used for both active design scheme. Uneven active device is easy to be controlled by Asymmetric S/D implant dose.

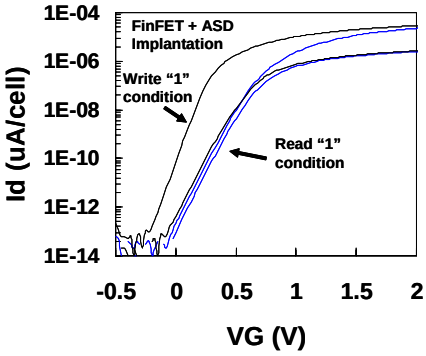

Fig. 7. Id-Vg characteristics of FinFET with ASD implantation. The Vt is lower for write "1" condition (storage node = low, bit line = high).

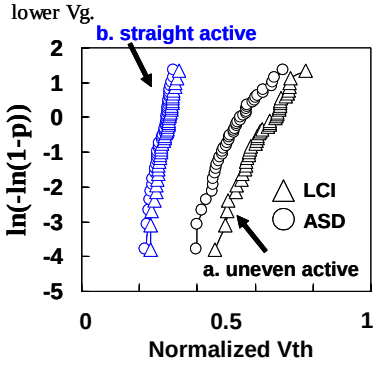

Fig. 8. V_T distribution of uneven and straight active with 2 different implant scheme (local channel and ASD implantation)

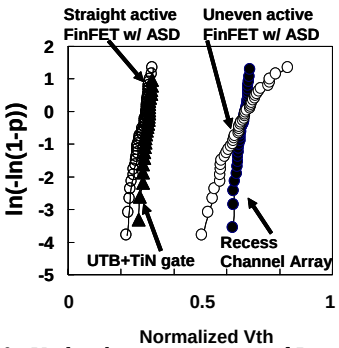

Fig. 9. V_T distribution Comparison of Recess channel array Tr., FinFET with asymmetric S/D and thin body Tr. with TiN gate. Uneven active device with ASD shows large distribution while recess channel, TiN gate UTB and straight active FinFET with ASD show negligible distribution.

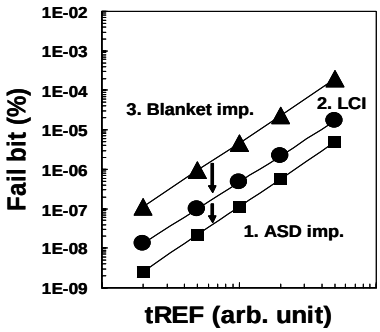

Fig. 10. Refresh characteristics of blanket implant, LCI (Local channel implantation) and ASD (Asymmetric S/D) implanted cell Tr. 512M FinFET DRAM.

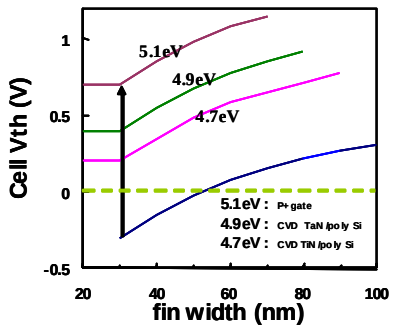

Fig. 11. V_T adjustment expectation of sub 40nm FinFET cell DRAM by using 4.7~5.1eV gate material such as CVD TiN, TaN and P+ gate.