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Application of HfSiON to Deep Trench Capacitors of Sub-45nm Node Embedded DRAM

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1. Abstract

ALD HfSiOx was applied to the node dielectric of deep trench (DT) capacitors of the 65nm node embedded DRAM (eDRAM) for the first time. As a result, capacitance enhancement of 30% from the conventional dielectric (NO) was achieved at the same level of leakage current. The main features of our ALD process are 1) a uniform thickness and depth profile of each component in DT by taking advantage of a catalytic effect of the precursors and 2) a reduced amount of impurities in the film without causing any degradation of step coverage.

2. Introduction

Over the last decade, a continuous trend in miniaturization of deep trench (DT) capacitors has required new technologies for maintaining a certain amount of capacitance per cell. Surface area enhancement techniques such as HSG or the application of Al2O3 to the node dielectric has been investigated [1]. As design rules edge into the sub-45nm region, however, geometrical options are exhausted because of physical limitations. Consequently, materials with an even higher dielectric constant than Al2O3 (~9) are required. Although HfSiON, which has been widely investigated as gate dielectric, shows both a higher k value (~13) and a thermal stability of up to 1000°C, it has never been considered as a candidate for the node dielectric of DT capacitors. This is due to the difficulty of depositing ternary materials into high aspect ratio structures with a uniform film composition.

3. Experiments

For ALD of HfSiOx, a method of alternate deposition of HfO2 and SiO2 is commonly used. On the other hand, the co-injection is a method of introducing multiple precursors into a chamber at the same time [2]. Fig. 1 schematically shows the procedure of the co-injection. Tetrakis(ethilmethylamino)-hafnium (TEMAHf) and Tetrakis(ethilmethylamino)silicon (TEMASi) are used as precursors for HfSiOx deposition. The Hf ratio (Hf/(Hf+Si)%) of the film can be controlled over the range 0~100% by varying precursor gas flows. Deposition rates (DR) of the co-injection as a function of the Hf ratio of the films are shown in Fig.2. The extremely low DR of SiO2 (<0.01nm/cycle) compared to HfO2 (~0.1nm/cycle) corresponds to the large disparity of sticking coefficients between TEMAHf and TEMASi. Then, the step coverage of HfO2 and SiO2 were evaluated with DT of the 65nm node embedded DRAM (eDRAM). As a result, the step coverage (bottom/top %) turned out to be approximately 60% for HfO2 and 0% for SiO2. This result suggests that bridging the difference of sticking coefficients is of paramount importance for a uniform depth profile of Hf/Si ratio in DT. In that connection, the DR enhancement from the proportional relationship between SiO2 and HfO2 was clearly observed for HfSiOx deposited by the co-injection (Fig.2). This phenomenon indicates a catalytic effect of TEMAHf in conjunction with TEMASi.

Nitridation of the HfSiOx films was performed by NH3 anneal. For the step coverage evaluation, DT of the 45nm node eDRAM was used. For the analysis of leakage mechanism, planer capacitors were fabricated with various ALD conditions. Also, DT capacitors were fabricated with the 65nm technology. Fig.3 shows the main part of the integration flow.

4. Results and Discussions

A. Step Coverage in DT (45nm node eDRAM)

Shown in Fig.4a-e are cross-sectional TEM images. Almost identical film thicknesses at the top and at the bottom of DT were confirmed. In addition, depth profiles of Hf and N of HfSiON fabricated by the alternate process (HfO2/SiO2) and the co-injection were obtained by SIMS (Fig.5). Almost uniform depth profiles of Hf and N were observed for the co-injection in contrast to the alternate process. Since the physical thickness of the film is confirmed to be almost constant in DT, the Hf/Si ratio of the film is deduced to be homogeneous in the depth direction. This difference can be attributed to the catalytic effect of the co-injection.

B. Mechanism of Leakage Current (Planer)

The relationship between the residual carbons from the precursors in the dielectric and the electrical properties of planer capacitors was examined. The carbon concentration was controlled by varying the substrate temperature during the ALD process. Shown in Fig.6 is the leakage current as a function of the carbon concentration measured by SIMS (EOT=3.5nm, 1V). As can be clearly seen from Fig.6, the residual carbons play a crucial role in the leakage current. The temperature dependence of the leakage current was also measured and the Arrhenius plot was obtained (Fig.7). A good linearity of the Arrhenius plot was observed, which indicates that the conduction mechanism is Poole-Frenkel (PF) type. In summary, reducing residual carbons directly leads to a lower PF current, which is a dominant mechanism.

By using higher substrate temperature and chamber pressure during the ALD process, the amount of carbon can be reduced. However, a severe degradation of step coverage, which was caused by thermal decomposition of the precursors, took place at a certain point.

C. Application to DT Capacitors (65nm node eDRAM)

For the purpose of fulfilling requirements for the step coverage and the reduction of impurities at the same time, a new ALD sequence was invented. The concept of SHO (Sequential High-pressure Ozone-treatment) is shown in Fig.8. The carbon reduction effect of SHO was confirmed by SIMS (Fig.9). Therefore, the co-injection combined with SHO at 4.5~9Torr was applied to DT capacitors of the 65nm node eDRAM. Shown in Fig.10 is a capacitance versus leakage current plot, which was measured at the operating voltage (Vcc/2 = 0.6V). The effect of SHO at a higher pressure was clearly observed and capacitance enhancement of 30% from the conventional dielectric (NO) was achieved at the same level of leakage current. A TDDB life time versus voltage plot measured at 85°C is shown in Fig. 11. The extrapolation to product area (dashed line) shows 10 years lifetime at 1.4V.

5. Conclusions

HfSiON was applied to the node dielectric of DT capacitors for the first time. The electrical properties of HfSiON showed the extendibility from the 65nm node eDRAM to the next generation. The step coverage was also confirmed to be almost conformal with DT of the 45nm node eDRAM. In conclusion, HfSiON by our newly developed ALD process is proved to be a promising candidate for the node dielectric of DT capacitors for the future generation.

References

[1] H. Seidl et al., IEDM Tech. Digest 2002, p.839
[2] Y. Senzaki et al., J. Vac. Sci. Tech. A 22(4), Jul/Aug 2004

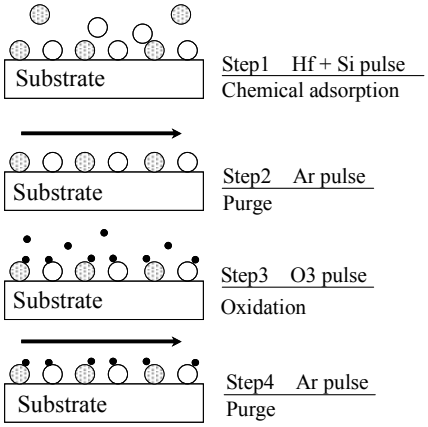


Fig.1 A procedure of the co-injection (1cycle).

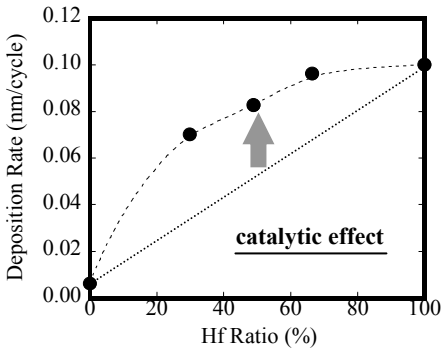


Fig.2 A plot of the deposition rate of the co-injection as a function of the Hf ratio.

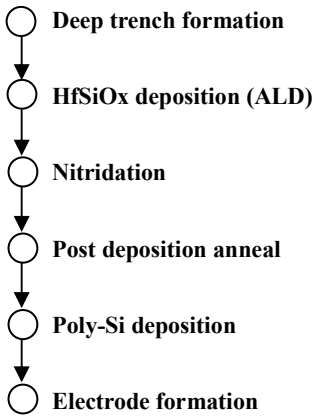
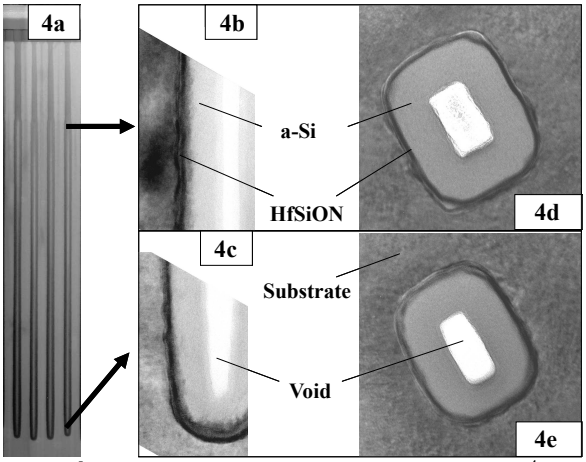


Fig.3 HfSiON integration flow.



TEM images of DT of the 45nm node eDRAM (AR > 50)

Fig.4a A whole image.

Fig.4b-c Perpendicular images to the wafer surface at the same magnification.

Fig.4d-e Parallel images to the wafer surface at the same magnification.

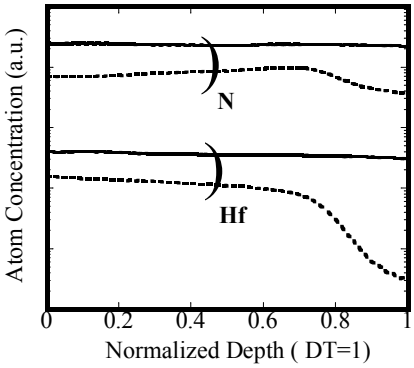


Fig.5 Depth profiles of Hf and N concentration by SIMS (solid : co-injection, dashed : alternate).

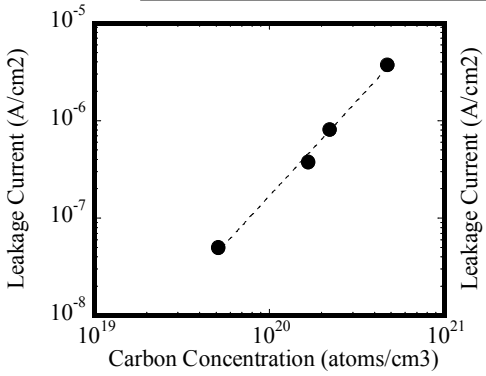


Fig.6 A plot of leakage current as a function of the carbon concentration (EOT=3.5nm, 1V).

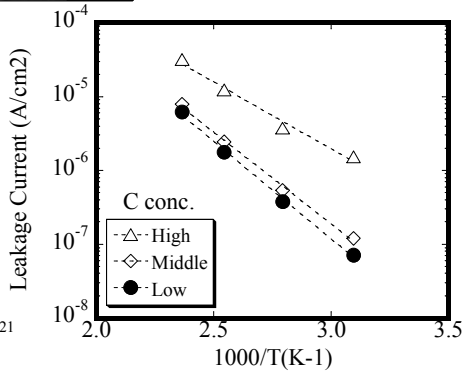


Fig.7 The Arrhenius plot of the samples with varied carbon concentrations.

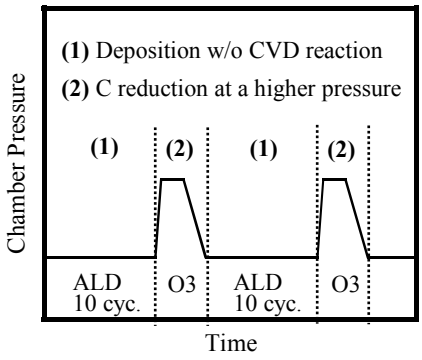


Fig.8 The concept of Sequential High-pressure Ozone-treatment (SHO).

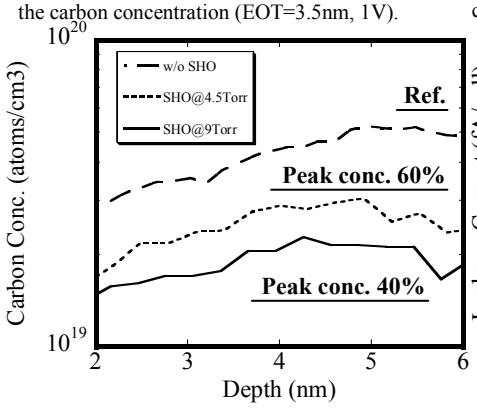


Fig.9 Depth profiles of the C concentration by SIMS, with and without SHO.

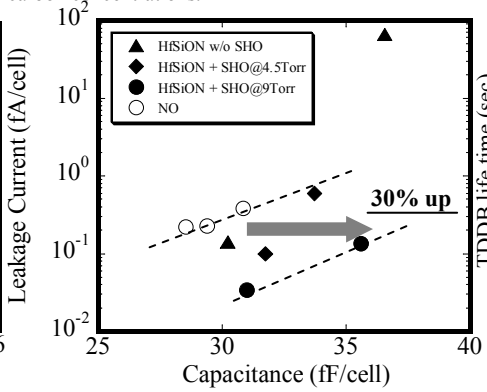


Fig.10 A capacitance versus leakage current plot (DT capacitors of the 65nm node eDRAM, 0.6V).

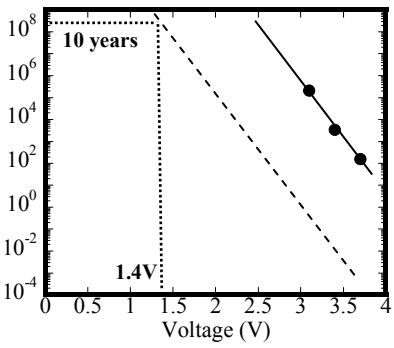


Fig.11 A TDDB life time versus voltage plot. The extrapolation to product area (dashed line) shows 10years lifetime at 1.4V.