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Improvement of Retention time by Hydrogen Penetration Slit in DRAM Integration with Triple Metallization

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Introduction

For high performance application of DRAM, the triple metallization plays a major role in determining the ease of design and the performance of DRAM circuit. The maximum benefit from the third level of the metal could be obtained by controlling the increased plasma damage due to additional integration processes. Even though high performance DRAM integration with multi-metallization is believed to be essential, its application to large diameter wafer process is limited because of plasma issues. Especially, the special care of retention time should be taken since the plasma damage is closely associated with the degradation of retention time. In a Recessed Cell Array Technology (RCAT) DRAM integration employing triple metallization, the reliability issue with respect to retention time is studied, and the overcoming method by alloying hydrogen (H_2) penetration slit is proposed in this paper.

Experimental

The triple metallization was implemented on 92nm RCAT DRAM technology, being quite stable in terms of maturity. Several experiments to prove the root mechanism in connection with the degradation of retention time were carried out. First, the difference between DRAM with double metal and triple metal was verified using test vehicle and real chip. Second, the partial area on triple metal was intentionally opend, and compared with the closed area in connection with retention time. Finally, three kinds of H_2 penetration slit on the third metal, were patterned and their impacts on retention time were evaluated.

Results and Discussion

Using test vehicle, the impact of multi-metallization is indirectly analyzed. RCAT pattern in test vehicle is highly susceptible to plasma damage categorized as the floating active-connected antenna. It has been reported that the plasma damages, with respect to floating junction, are pronounced through the exposed active area of antennas connected. Also, effective plasma charges are determined by the exposed active area [1]-[3]. Instant plasma (+) charging at the floated active (gate to overlapped active) causes electron injection from polysilicon into gate oxide, finally leading to trapped electrons in the upper position of gate SiO_2. Since instant plasma charge injection increase with the additional increase of plasma processes, multi-metallization scheme becomes critical. With regard to cell transistor behavior after *dc* Fowler-Nordheim (FN) stress, two metallization schemes are compared in test vehicle level (Fig.1). Threshold voltage (Vth) of cell with triple metal decreases, and off-leakage incrases considerably under static *dc* FN stressing. Whereas, Vth of cell with double metal increases in opposite direction, and the increase of off-leakage is relatively smaller. Since the application of FN field enables electrons (trapped on upper position of SiO_2) to discharge easily into gate electrode, I-V curve shifts in a negative direction. In the test vehicle level, the severe degradation of cell with triple metal comes from increased plasma damage due to additional plasma processes and insufficient alloying effect due to lengthened H_2 penetration path. The characterized results of gate induced drain leakage (GIDL) and junction leakage on 90K cell array pattern are shown in Fig.2. The considerable increase of GIDL and junction leakage is obvious in cell pattern with triple metallization. If the situation is not completely identical and the degree of plasma damage is different, both the increase of additional plasma processes and lengthened H_2 penetration path still remains affected in real chip. Real cells with triple metal have a difficulty in releasing the damaged Si/SiO_2 interface by H_2 alloying. Fig.3 shows the dependence of retention time on metallization scheme. Decrease of retention time for DRAM with triple metal is remarkable, which is in a good agreement with characterized results in test vehicle level. In order to clarify its mechanism, the partial area on triple metal is intentionally opend on same chip, and compared with the closed area from the viewpoint of retention time. Based on the severe creteria(1s) of X-march retention time, failure bits of DRAM with partial open area on the third metal are relatively smaller as shown in Fig.4. Finally, the formation of H_2 penetration slit on third metal is considered as its solution. Impact of H_2 penetration slit shape on retention time is shown in Fig.5. Larger opened slit promotes the alloying efficiency, resulting in dramatic improvement of retention time, which is shown in cumulative percent plot of failure bits, based on the given creteria of retention time. Summarizing afore-mentioned results, our proposed model is well consistent with experimental results.

Conclusion

The degradation of retention time is found in RCAT DRAM integration employing triple metallization, which is responsible for the increased plasma damage due to additional plasma processes and insufficient alloying effect due to lengthened H_2 penetration path. The formation of H_2 penetration slit on the third metal is considered as its solution.

References

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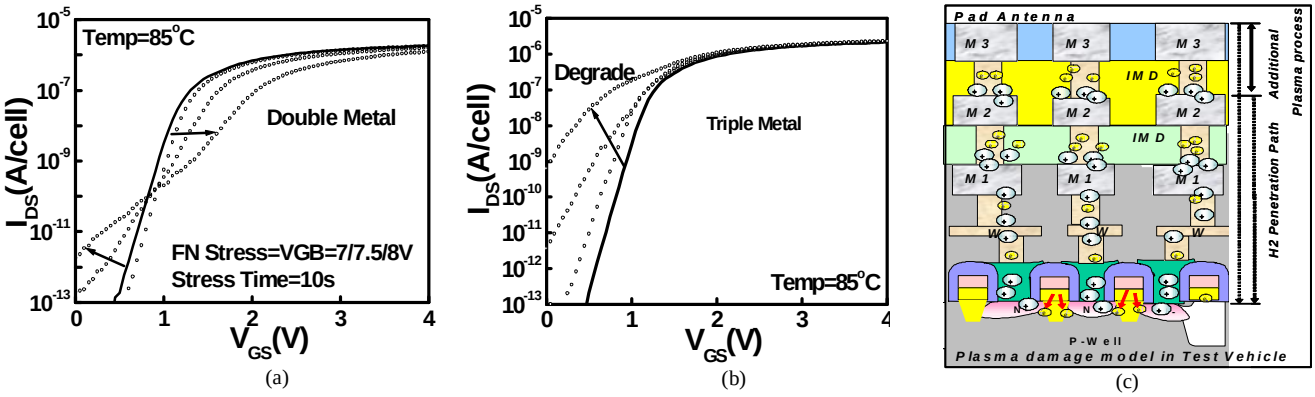
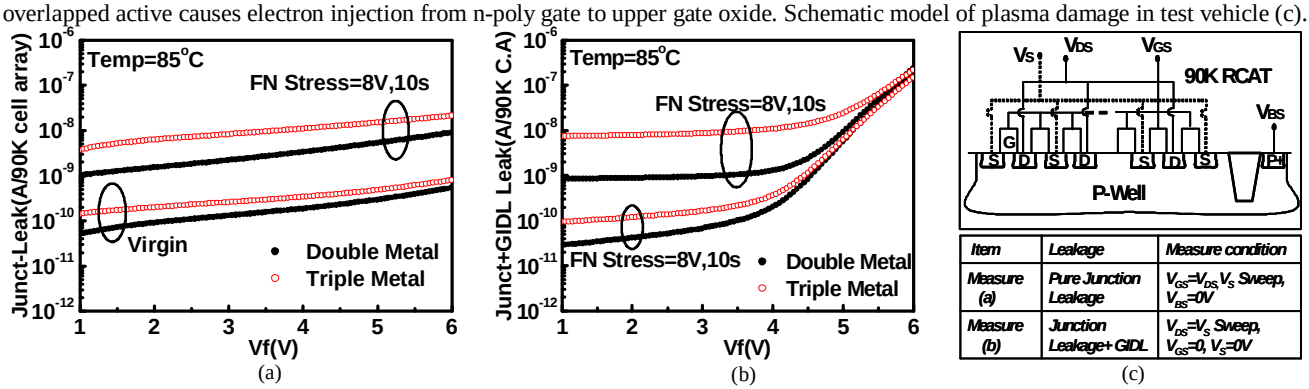


Fig. 1 Comparison of cell transistor behavior under dc FN stressing between cell with double metal(a) and triple metal(b). In test vehicle level, the severe degradation of cell with triple metal comes from the increased plasma damage due to additional plasma processes and the insufficient alloying effect due to lengthened H_2 penetration path. Since the application of FN field enables electrons (trapped on upper position of SiO_2) to discharge easily into gate electrode, I-V curve shifts in a negative direction. Instant potential increase of gate to overlapped active causes electron injection from n-poly gate to upper gate oxide. Schematic model of plasma damage in test vehicle (c).



Item	Leakage	Measure condition
Measure (a)	Pure Junction Leakage	$V_{GS}=V_{DS}$ V_S Sweep, $V_{BS}=0V$
Measure (b)	Junction Leakage+ GIDL	$V_{DS}=V_S$ Sweep, $V_{GS}=0$, $V_S=0V$

Fig. 2 Characterization of GIDL and junction leakage on 90K cell array pattern. Pure Junction lekage (a), Junction leakage + GIDL(b) and schematic view of measuring method(c). GIDL and junction leakage is closely assiciated with the decrease of retention time of DRAM with triple metallization.

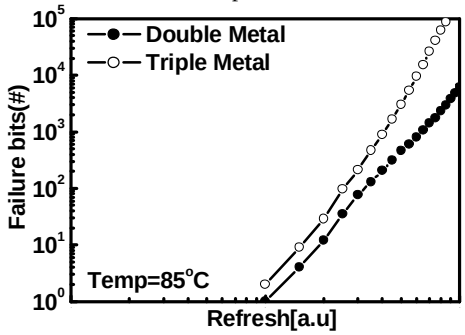


Fig.3 Comparison of static retention time. Retention time for DRAM with triple metal is worse than that with double metal.

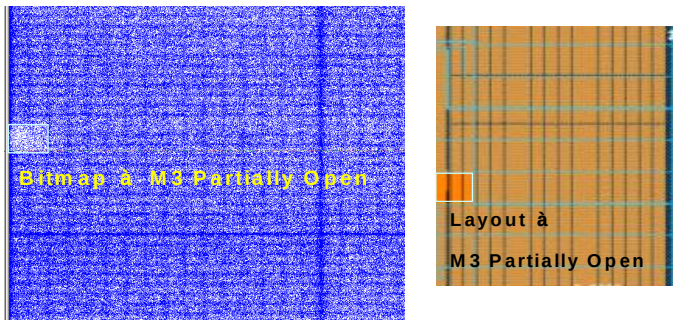


Fig.4 Based on the severe creteria(1s) of X-march static retention time, failure bits of DRAM with partial open area on triple metal are relatively smaller.

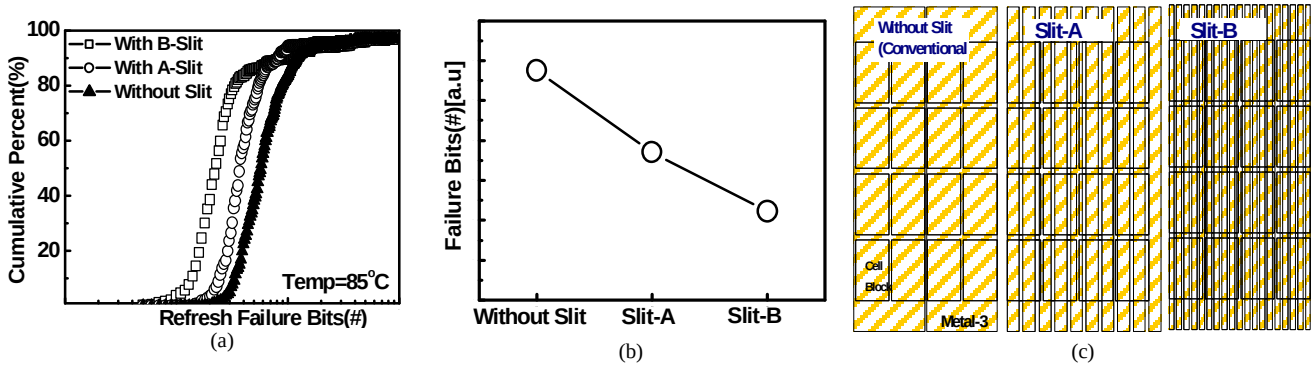


Fig.5 Size impact of H_2 penetration slit on retention time is shown in Fig.5. Larger slit promotes the alloying efficiency, resulting in dramatic improvement of retention time. Cumulative percent of failure bits, based on the given creteria of X-march static retention time(a). Value plot that corresponds to 50% failure bits(b). Schematic view of slit type(c).