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Lower Power and Higher Speed Operations of Phase-Change Memory Device Using Antimony Selenide (Sb_xSe_{1-x})

Sung-Min Yoon[1], Nam-Yeal Lee[1], Sang-Ouk Ryu[1], Kyu-Jeong Choi[1], Young-Sam Park[1], Seung-Yun Lee[1], Byoung-Gon Yu[1], Myung-Jin Kang[2], Se-Young Choi[2] and Matthias Wuttig[3]

[1]Basic Research Laboratory, Electronics & Telecommunications Research Institute (ETRI), 161 Gajeong-dong, Yuseong-gu, Deajeon 305-350, Korea
Phone: +82-42-860-6293, Fax: +82-42-860-5608, E-mail: sungmin@etri.re.kr
[2]Department of Ceramic Engineering, Yonsei University, Seoul 120-749, Korea
[3]Physikalisches Institut der RWTH Aachen, D-52056 Aachen, Germany

1. Introduction

In the present highly-developed information-oriented society, the advent of the Unified-Memory equipped with almighty functions such as low power, high speed, robust endurability, and nonvolatility are being strongly demanded. The PRAM (Phase-Change Random Access Memory) is one of the most promising candidates for the next-generation unified-memory due to its excellent logic compatibility, scaling-favorable operation scheme, and low fabrication cost [1-2]. The PRAM utilizes the reversible phase change phenomena between crystalline and amorphous states of chalcogenide materials by electrical resistive joule heating. The resistance of the crystalline phase (SET) is much lower than that of the amorphous phase (RESET). This resistance difference between the two states is known as more than three orders of magnitude, which provides a sufficient data sensing margin for the memory operations [3].

In PRAM applications, the amplitude of current pulse and the duration of pulse width for the stable phase-change operations are supposed to be two major concerns, since they are directly related to the low-power and high-speed operations. So far, a chalcogenide metal alloy of $Ge_2Sb_2Te_5$ (GST) has been mainly employed for the fabrication of PRAM [4-5]. Actually, GST is one of the most well-known chalcogenide materials, since it has been used for the commercial rewritable optical storage disk products, which utilize laser-induced structural phase changes in the GST layers. Although the PRAM device using GST has shown a kind of excellent functionalities in the proto-type chips, the introduction of new material is indispensable for the realization of future higher-density PRAM comparable to Flash memory, since GST has a relatively high melting temperature (T_m=620℃).

In this study, we fabricated the phase-change device using new chalcogenide material of antimony selenide (Sb_xSe_{1-x}). We confirmed the feasibility of newly fabricated device by comparing to the conventional device using GST. The obtained results are very promising for lower power and higher speed operations of phase-change memory devices.

2. Antimony Selenide Phase-Change Material

Sb_xSe_{1-x} has been also researched for the application of optical storage disks [6-7]. Although this material was not applied for practical products due to a few drawbacks, lower T_m (about 540~560℃) is very beneficial factor for PRAM devices. Fig. 1(a) shows the change of sheet resistance (R_s) as a function of temperature. The heating rate was set to be 5 K/min. The composition x of Sb_xSe_{1-x} varied to 60, 65, and 70. The values of R_s for all compositions experienced the drastic change from about 10 MΩ/□ to about 100 Ω/□. The temperature points where abrupt decrease of R_s occurs can be obtained by plotting the dR_s/dT, as shown in Fig. 1(b), in which the local minima of plots correspond to crystallization temperature (T_c). For example, the measured T_c of 122℃ for $Sb_{70}Se_{30}$ was supposed to be too low for the reliable device operations.

Fig. 2 shows the Power-Transition-Effect (PTE) diagrams of GST and $Sb_{65}Se_{35}$, in which we can evaluate the required time (t_c) for crystallization of given materials in rough way. The contrast (color) in PTE diagram describes the degree of crystallization. The brighter contrast (yellow or red in color) of part I for $Sb_{65}Se_{35}$ says that the t_c of $Sb_{65}Se_{35}$ is much faster than that of GST. We also confirmed by PTE diagrams that t_c was reduced as the increase of Sb composition. Considering the values of T_c and t_c for various compositions, we selected the $Sb_{65}Se_{35}$ for the fabrication of phase-change memory devices.

3. Fabrication of Phase-Change Memory Devices

The fabrication procedures for the phase-change memory devices using $Sb_{65}Se_{35}$ and GST are as follows. Firstly, bottom electrode contact (BEC) of TiN/TiW was formed on SiO_2/Si substrate, on which SiO_2 insulation layer was deposited by PECVD at 400℃. Active pores for the contact between chalcogenide and BEC were patterned into SiO_2 layer by dry etching method, in which the contact size was designed to be 0.5 μm. Then, GST or $Sb_{65}Se_{35}$ was deposited by RF magnetron sputtering method and molecular beam epitaxy (MBE), respectively. On these structures, oxide passivation layer was formed by ECR-CVD at room temperature. Finally, top electrode contact (TEC) of W was formed on chalcogenide layers, after the via-contact was patterned. Fig. 3 shows a schematic cross-section and a photograph of the fabricated memory device.

4. Comparisons of Operation Behaviors between GST and $Sb_{65}Se_{35}$ Devices

The BEC size (0.5 μm) of the fabricated device in this study is supposed to be still too big to anticipate the practical level device operations. Therefore, we made comparisons of operation behaviors between GST and $Sb_{65}Se_{35}$ devices in order to confirm the feasibility of proposed new chalcogenide material.

The SET-RESET operations of fabricated devices were measured as a function of applied pulse width when the amplitude of voltage pulse was 5 V. The required times for RESET (t_{RESET}) and SET (t_{SET}) operations of GST device were observed to be 50 ns and 1 μs, respectively, as shown in Fig. 4(a), while those of $Sb_{65}Se_{35}$ device were 35 ns and 250 ns. This suggests that the $Sb_{65}Se_{35}$ device can operate with higher speed than GST device, which is related to the fast crystallization speed of $Sb_{65}Se_{35}$. Fig. 5 and Fig. 6 show the programming curves (R-I) for the SET and RESET operations of fabricated devices, respectively. The current pulses with various amplitudes were applied for data programming. The current values for SET (I_{SET}) and RESET (I_{RESET}) operations of $Sb_{65}Se_{35}$ device were observed to be smaller than those of GST device. Especially, I_{RESET} decreased from 15 mA (GST) to 1.6 mA ($Sb_{65}Se_{35}$), when the pulse width was fixed at 100 ns. This reduction of I_{RESET} is due to the lower T_m of $Sb_{65}Se_{35}$ and will contribute to the lower power operation of PRAM.

5. Conclusion

We proposed a new chalcogenide material of $Sb_{65}Se_{35}$ for the PRAM applications. It was confirmed that the phase-change memory device using $Sb_{65}Se_{35}$ showed shorter t_{SET} and smaller I_{RESET}, comparing to the device using GST. From the obtained results, we can conclude that $Sb_{65}Se_{35}$ is one of the most promising materials for the high-density PRAM with lower power and higher speed operations.

Acknowledgements

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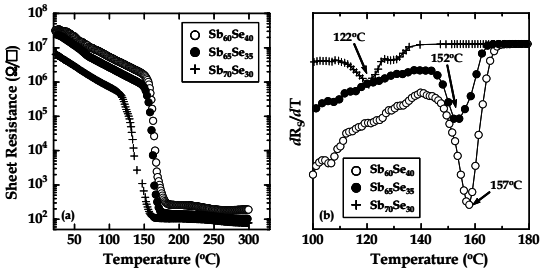

Fig. 1 (a) Sheet resistance (R_s) of Sb_xSe_{1-x} as a function of temperature. (b) Derivative of R_s.

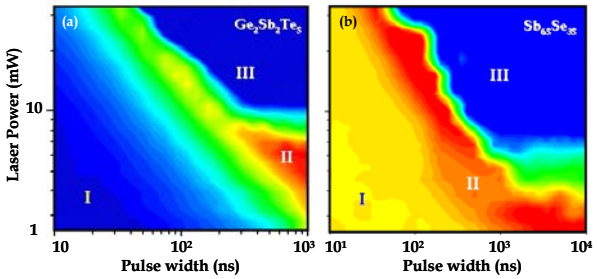

Fig. 2 PTE diagrams of (a) GST and (b) $Sb_{65}Se_{35}$.

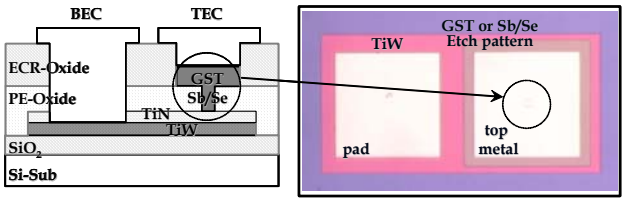

Fig. 3 (a) Schematic diagram of cross-section and (b) photograph of fabricated device.

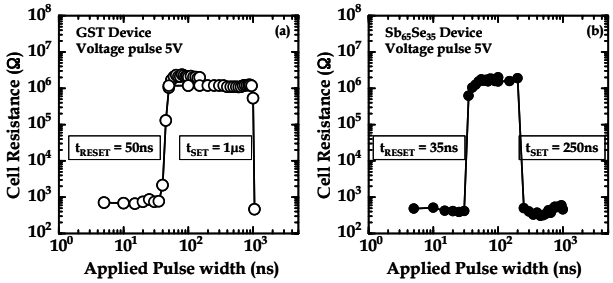

Fig. 4 Resistance variations of phase-change memory devices using (a) GST and (b) $Sb_{65}Se_{35}$ as a function of pulse width when the voltage pulse of 5 V was applied.

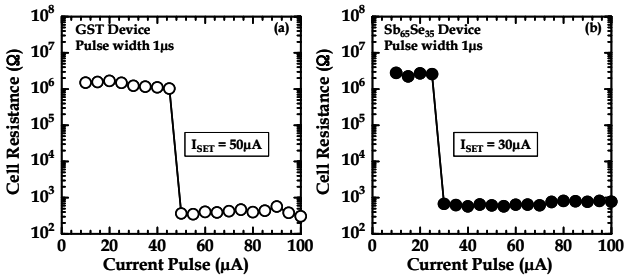

Fig. 5 SET programming curves (R-I) of devices using (a) GST and (b) $Sb_{65}Se_{35}$ when the current pulse with 1 μs was applied.

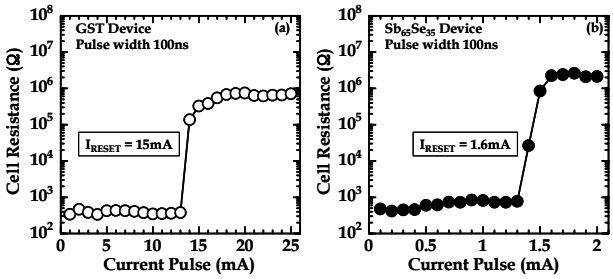

Fig. 6 RESET programming curves (R-I) of devices using (a) GST and (b) $Sb_{65}Se_{35}$ when the current pulse with 100 ns was applied.