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Study of Temperature Effect on Low V_T State Behavior of NBit Cells

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Abstract —The **low threshold voltage (V_T) state** behavior of an Nbit cell is investigated. At room temperature (R. T.), the erase V_T will drift up with increasing retention time, which follows the famous tunneling front model, and gets worse as the effective channel length (L_{eff}) scales down. However, at high temperature, the erase V_T will drift either ways (up/down) with increasing retention time depending on the L_{eff} of the test samples. According to our simulation results, the lateral movement of holes, which is accelerated by high T baking, is suspected to be the root cause.

I. Introduction

The reliability issues of an NBit cell, which uses a nitride film as a charge storage material, have been received much attention recently. A V_G acceleration method [1] and a temperature acceleration test [2] are proposed for qualification of the NBit devices in its program state. As for the low V_T states, the hole detrapping in a stressed bottom oxide [1] and the lateral migration of trapped holes in the nitride [3] are proposed. In this paper, we focus on the reliability issues at the low V_T states and both single cells and product are studied. By varying the bake temperature and the L_{eff} of test samples, the responsible mechanisms for each case are identified.

II. Experimental Results

As reported in [4,5], R. T. drift is pronounced already after the first program/erase (P/E) cycle and reaches a weakly pronounced maximum at 10-100 cycles. Thus, during experiments, 100 P/E cycled cells or products are chosen. After cycling, the erase V_T of a single cell and the high bound of product erase state V_T distribution are recorded, and the V_T variations (ΔV_T) with retention time are then plotted on a semi-log scale as shown in Fig. 1. The sample is firstly stored at R. T. for 100 hours and then baked at 150°C for another 24 hours. For both samples, the ΔV_T is firstly follows a straight line and then abruptly drifts up after bake. The linearity of ΔV_T at R. T. can be explained by the tunneling front model [1], ***but the abrupt increase at high temperature is observed for the first time***. This result contradicts with our previous observation shown in [3], which claims that the low V_T states will drift down after high T bakes. To clarify such phenomena, cells, which are fabricated by 0.25μm and 0.13μm technologies, are studied. Two of them experienced 100 P/E cycles and then stored at R. T. The other two performed erase stress only and then are baked in the oven. In Fig. 2, at R. T., a straight line is observed for both channel length and the slope is higher for a shorter channel length. On the other hand, for those baked in oven, the V_T drifts down for the cell with longer channel length but drifts up for the other. These results imply that cells at R. T. and high T exhibit different drift mechanisms.

III Discussions

According to [1] and [3], hole tunneling should dominate the R. T. drift and hole lateral migration should be responsible for the high T drift. Based on this knowledge, the observed channel length- and temperature- dependence are explained as follows. In Fig.3, the erase characteristics of cells with L_G=0.32μm and L_G=0.26μm are shown. The erase speed of both cells is similar except that the erase VT is almost saturated for L_G=0.32μm while an over-erasure occurs at a shorter L_G. This result suggests that the injection width of band-to-band tunneling induced hot hole is controlled by lateral field (the applied V_D during erase) and is insensitive to L_G [2]. Since the occupational ratio of hole stressed area is increased, the magnitude of R. T. drift is also affected. In Fig. 4, the slope of the R. T. drift is plotted against the L_G and the corresponding punch through voltage (V_{PT}) is also shown. It is clearly observed that the slope drastically increased once the V_{PT} starts to decrease. As for the cells under high T bake, it is curious why two different behaviors are observed as channel length scales. Thus, in Fig. 5(a), a uniform hole distribution is applied for simulation with various peak density while keeping the volume of holes constant to emulate the lateral migration. In Fig. 5(b), two different behaviors are successfully re-produced, which is in agreement with the experiment results. The potential distribution of the two cases under read operation is plotted in Fig. 6 (a) and Fig. 6(b). It is found that the V_T starts to drift up once the main channel potential is fully controlled by the stored holes.

IV Conclusions

The low V_T state behavior of NBit cells is reviewed. It is found that the hole tunneling induced V_T drift up is pronounced at room temperature especially when the channel length further scales. However, the lateral migration of holes, which may causes the low V_T state drift up or down depending on the channel length, will be observed after high temperature bake. Since the responsible mechanism is different at different temperature, the qualification method should be different for them.

References:

[1] W. J. Tsai et al., *IEEE IRPS*, p. 34, 2002
[2] M. Janai, *IEEE IRPS*, p. 102, 2003
[3] N. K. Zous et al., *IEEE EDL*, p. 649, 2004
[4] Y. Roizin et al., *IEEE EDL*, p. 35, 2005
[5] T. Wang et al., *IEEE IEDM*, p. 741, 2003

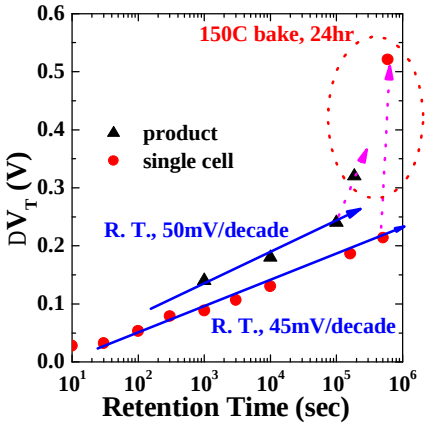


Fig. 1 The retention time evolution of low V_T states. The sample is firstly stored at R. T. for 100 hours and then baked at 150°C for another 24 hours.

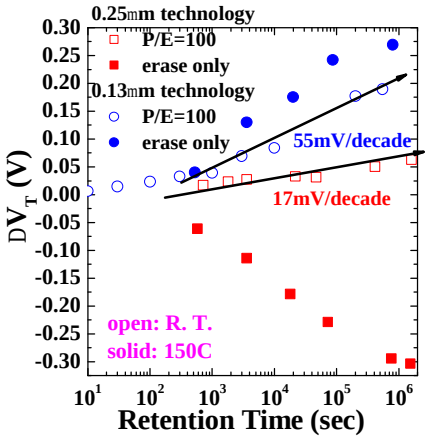


Fig. 2 Samples with 100 P/E cycles are stored at R. T. and those with erase only operation are baked at 150C.

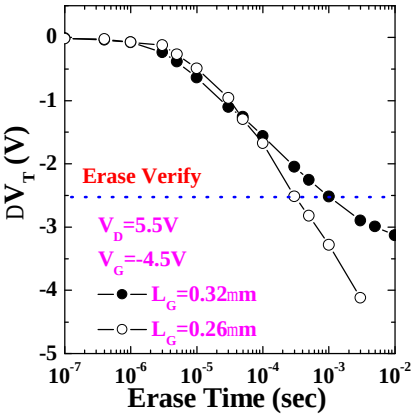


Fig. 3 The erase characteristics of two channel lengths. To pass the erase verify level, a similar erase time is required.

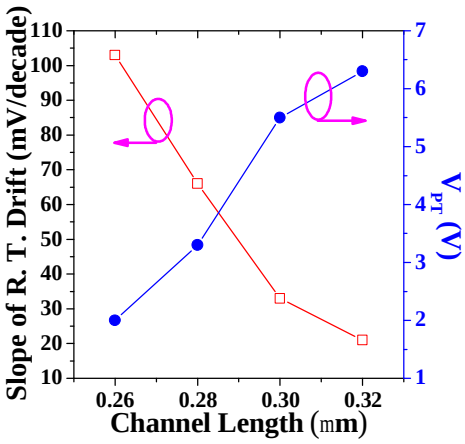
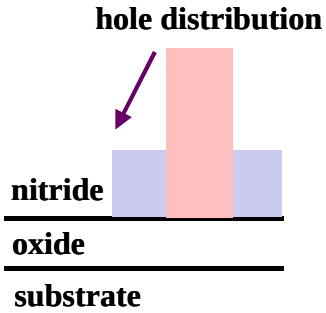


Fig. 4 The channel length dependence of the slope of R. T. drift. The V_{PT} versus channel length is also shown.



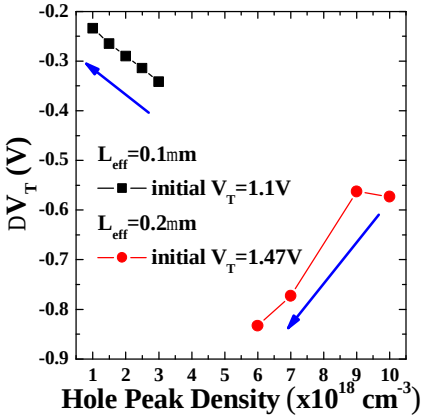


Fig. 5 (a) Schematic illustration of the hole lateral migration in the nitride layer. (b) The hole peak density evolution of the DV_T for L_{eff}=0.1mm and L_{eff}=0.2mm is simulated. During simulation, the total volume of holes is kept constant.

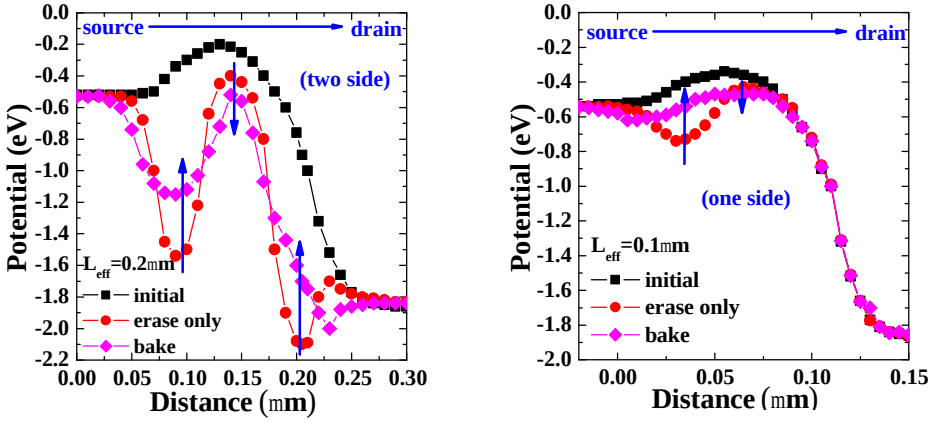


Fig. 6 Corresponding to Fig. 5, the potential evolution along the channel length is plotted for three states including initial, erase only, and after bake. (a) L_{eff}=0.2mm with two sided hole distribution. (b) L_{eff}=0.1mm with one sided hole distribution.