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NeoFlash® - True Logic Based 0.18μm Single Poly Embedded SONOS Flash

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Abstract – A new simple and low cost logic based 0.18μm single poly 2T p-channel embedded SONOS Flash (NeoFlash®) with fast programming and high reliability is demonstrated in this paper. With merely 3 additional non-critical masks, this device has been successfully embedded into 0.18μm CMOS logic process. Hot electron injection is utilized to achieve fast programming. Uniform channel tunneling erasure and hot-hole-free operation scheme reinforce reliability as well as endurance characteristics. Due to the simplicity in both process and design, small chip area of 2.93mm^2 (cell size 0.76μm^2) is achieved for 2Mbit embedded Flash. Performance of a 2Mbit array proves the great feasibility of this new embedded SONOS Flash.

I. Introduction

Due to superiority in process simplicity, structure scalability and charge retention characteristics, SONOS technology has been considered as a great substitution for floating gate nonvolatile memory, especially in embedded applications [1]. Along with the improvement in device structure and ONO film growing process, operations of a SONOS device have been comprehensively developed [2, 3]. Injecting electrons into the nitride layer can be achieved with either channel tunneling or hot electron injection (HEI). Eliminating electrons inside the nitride layer is generally done by hot hole injection (HHI). However, hot hole injection raises instability issues such as oxide damage, overerase and unexpected charge loss/gain [4]. To overcome these problems, we developed NeoFlash, a 2T p-channel embedded SONOS Flash utilizing hot electron injection for fast programming and channel tunneling for uniform erasing. Hot electron injection efficiency in p-channel devices can be higher than in n-channel devices [5, 6]. Furthermore, channel tunneling erase in p-channel device does not produce hot hole injection because of the larger hole barrier height [7]. The hot-hole-free operation scheme in proposed p-channel device further reinforces the reliability of our newly developed embedded SONOS Flash.

II. Device and Process

Following the minimum design rules of 0.18μm logic process, schematic layout and cross sectional view of a single NeoFlash bitcell are demonstrated in Fig. 1. Each bitcell consists of two p-channel transistors in series; one is the thick-gate transistor for selection, and the other is the SONOS transistor for data storage. When programming the cell, a high bitline voltage is employed to result in hot hole induced hot electron injection into the nitride layer. To erase the cell, a negative voltage on the memory cell gate and a positive voltage on N-well/BL/SL are applied to induce the out-tunneling of electrons stored in the nitride layer. Bitcell at program state has high conductivity and can drive large current under read operation. SEM cross sectional view of a NeoFlash NOR type array and TEM picture of the SONOS transistor are demonstrated in Fig. 2. Effective oxide thickness of the ONO stack is well controlled around 100Å to ensure low voltage operations. To embed NeoFlash into CMOS logic process, only three additional non-critical masking layers are required, as listed in table 1. Because of the low voltage operation scheme, there is no need for HV-related processing indispensable in other embedded nonvolatile memory technologies. Decreased number of masking layers, simple single poly process steps and reduced high voltage module areas consequently lead to significant cost savings and yield improvement for this embedded SONOS Flash. Listed in table 2 are the key features of NeoFlash bitcell and 2Mb chip.

III. Results and Discussion

Characteristics of the CMOS logic devices processed with NeoFlash-related steps are compared with their pure logic SPICE models in Fig. 3. The IV curves are approximately identical, indicating the embedded SONOS process does not impact on logic CMOS devices. Operation conditions of a NeoFlash bitcell are illustrated in Fig. 4. The select transistor switches for bitcell selection during programming and read. Erasing bias is divided between memory cell's gate and other terminals, and the highest bias level does not exceed 6V. Consequently, periphery decoding and charge pumping circuitry can be scaled and simplified significantly. Programming characteristics under various bitline biases are compared in Fig. 5. The bitcell can be programmed to the desired program state in 10μs with a maximum voltage of 6V. Even when there is broad distribution of initial state as illustrated in Fig. 6, the trends under fixed programming condition expeditiously merge during the programming process. Channel tunneling erasing characteristics as a function of memory cell's gate voltage are demonstrated in Fig. 7. With 12V across the ONO stack, the bitcell can be successfully erased within 500ms. Even when the initial current level varies largely, the erasing trends merge after 100ms in Fig. 8. The self-convergent phenomenon in both programming and erasing trends can contribute to tight state distribution. The endurance characteristics of NeoFlash are illustrated in Fig. 9. Not only the program/erase states are stable within 10K cycles, operation window expands with cycling count. In comparison with the window drift and closure issues commonly addressed in HEI programming/HHI erasing applications, NeoFlash demonstrates satisfactory P/E cycling endurance characteristics. With regard to program disturb illustrated in Fig.10, an unselected NeoFlash bitcell can hold unaffected more than 5,000 times of programming, which is hundreds more times longer than required in normal array operation. Functional lifetime with regard to read disturb is illustrated in Fig. 11. Under an extremely critical criterion, NeoFlash bitcell can achieve continuous read for more than 10 years under 1.8V read operation. Charge retention performance of a 2Mb NeoFlash chip under 150°C, 200°C and 250°C is demonstrated in Fig. 12. In comparison with the industrial standard of 1000hr@150°C for 30% degradation equivalent to 10years@85°C, NeoFlash demonstrates good retentivity. Endurance characteristics of a 2Mb NeoFlash chip are shown in Fig. 13. No tail bit is observed as expected, since SONOS device is known for its immunity against local defects.

IV. Conclusion

In this paper, a new simple and low cost logic based 0.18μm single poly 2T p-channel embedded SONOS Flash with fast programming and high reliability is demonstrated. Only 3 additional masks are required besides baseline logic process, and very little effect is observed on original CMOS devices. Hot electron injection can shorten the programming time to tens of microseconds for emerging high speed and high density applications. Hot-hole-free channel tunneling lead to uniform erasure with high reliability. Program disturb and read disturb are not issues of concern. Charge retention performance is sufficient for 10 years at 85°C. No tail bit after programming and erasing is observed. NeoFlash is very promising for embedded Flash in system on chip (SoC) applications due to its simple process, design and low cost.

V. Reference

[1] C. Swift et al, *IEDM Tech. Dig.*, p.927, 2002
[2] T. Chan et al, *IEEE Elec. Dev. Lett.*, Vol.8, p.93, 1987
[3] B. Eitan et al, *IEEE Elec. Dev. Lett.*, Vol.21, p.543, 2000
[4] W. Tsai etal, *IEDM Tech. Dig.*, p.719, 2001
[5] C. Hsu et al, *Intl. Conf. Sol. State Dev. and Mat.,* p.140, 1992
[6] C. Hu, *VLSI Elec.*, Vol.18, p.119, 1989
[7] K. Ng et al, *IEEE Tran. Elec. Dev.*, ED-30, p.871, 1983

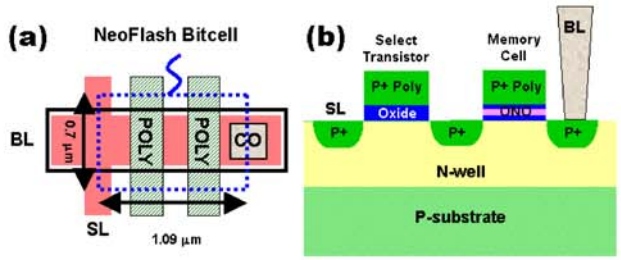

Fig. 1 (a) Schematic layout and (b) cross sectional view of a NeoFlash bitcell

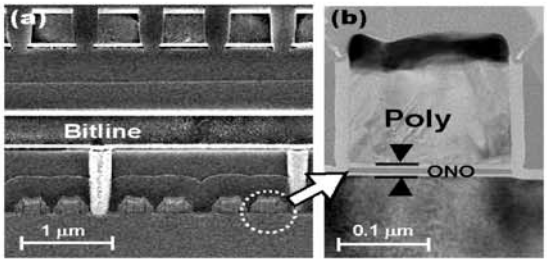

Fig. 2 (a) SEM cross sectional view of NeoFlash NOR type array along the bitline direction and (b) TEM cross sectional view of the SONOS memory cell

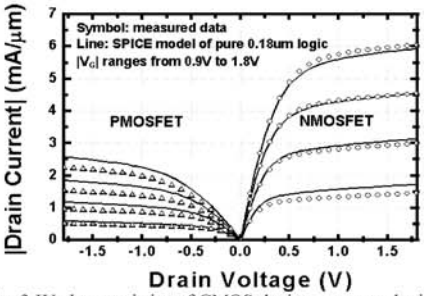

Fig. 3 IV characteristics of CMOS devices processed with SONOS-related steps vs. pure logic SPICE models

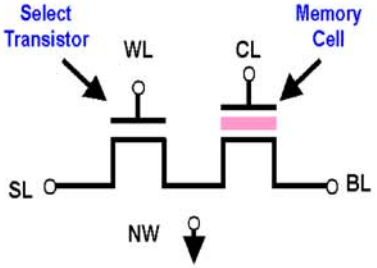

Fig. 4 Schematic and operation conditions of a NeoFlash bitcell

Unit: V

Operation	Terminal	WL	CL	BL	SL	NW
Program	Selected	-4.5	-1	-6	0	0
	Unselected	0	-1	-6	0	0
Erase	Selected	3.3	-6	6	6	6
	Unselected	3.3	0	0	0	0
Read	Selected	-3.3	0	-1.8	0	0
	Unselected	0	0	-1.8	0	0

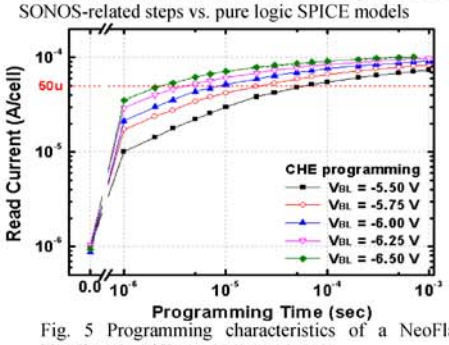

Fig. 5 Programming characteristics of a NeoFlash bitcell under different bitline voltages

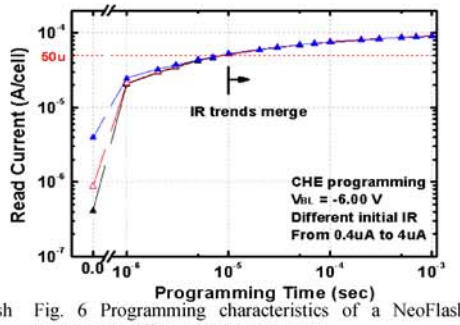

Fig. 6 Programming characteristics of a NeoFlash bitcell with different initial ERS states

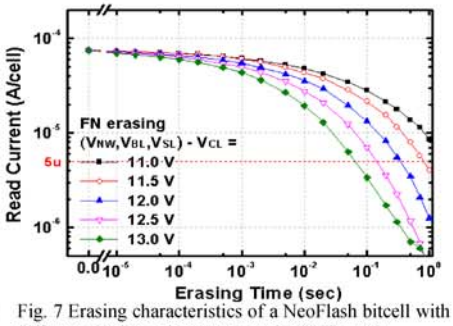

Fig. 7 Erasing characteristics of a NeoFlash bitcell with different erasing voltages across the ONO stack

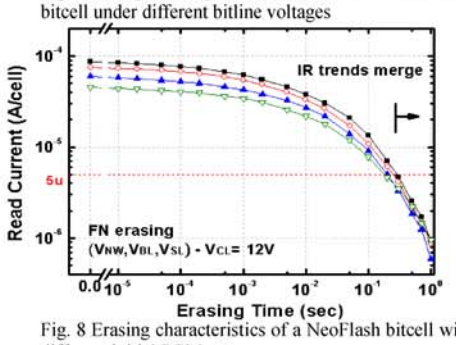

Fig. 8 Erasing characteristics of a NeoFlash bitcell with different initial PGM states

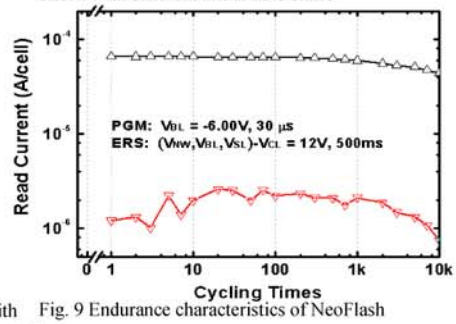

Fig. 9 Endurance characteristics of NeoFlash

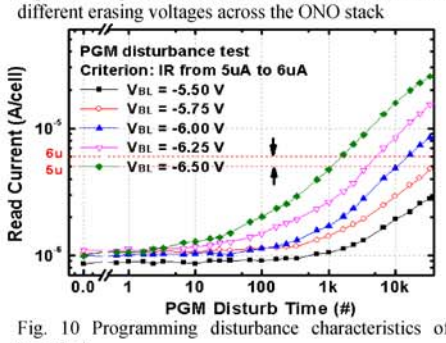

Fig. 10 Programming disturbance characteristics of NeoFlash

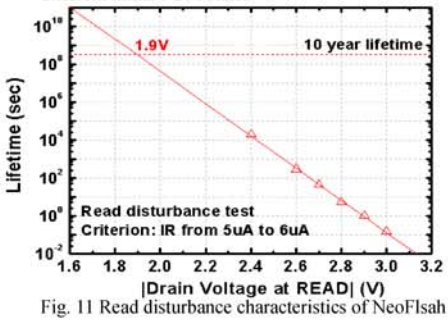

Fig. 11 Read disturbance characteristics of NeoFlsah

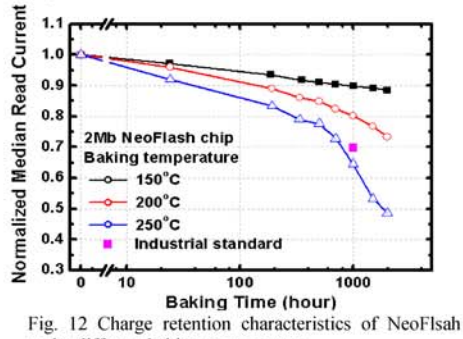

Fig. 12 Charge retention characteristics of NeoFlsah under different baking temperatures

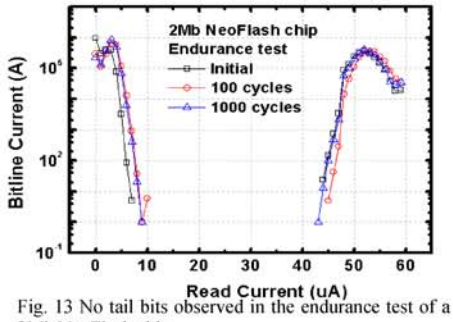

Fig. 13 No tail bits observed in the endurance test of a 2Mb NeoFlash chip

Table 1 Process comparison

Process step	CMOS logic	CMOS + NeoFlash
Isolation	✓	✓
➡ *Deep nwell formation*		+1 mask
Logic well formation	✓	✓
➡ *ONO film deposition*		✓
➡ *ONO patterning*		+1 mask
Logic gate oxidation	✓	✓
Poly gate deposition	✓	✓
Poly gate patterning	✓	✓
➡ *Residual ONO removal*		+1 mask
LDD implant	✓	✓
S/D formation	✓	✓
Backend process	✓	✓
Additional masking steps	-	+3

Table 2 Key features of NeoFlash bitcell and chip

Category	Item	Specification
NeoFlash Bitcell	Cell Size	0.763um²
	Program Time	30μs
	Erase Time	500ms
	Program Voltage / Current	6V / < 200μA
	Erase Voltage / Current	12V / <100nA
NeoFlash Chip	Operating Voltage	3.3V/1.8V
	Operating Temperature	-40°C ~ 125°C
	Program Mode	Byte Program
	Erase Mode	Chip/Sector Erase
	Access Time	< 40ns
	Data Retention	10 year @ 85°C
	Endurance	At least 1K cycles